

# **CSC 252: Computer Organization**

## **Fall 2021: Lecture 14**

Processor Architecture:  
Pipeline dependencies

Instructor: Alan Beadle

Department of Computer Science  
University of Rochester

# Announcements

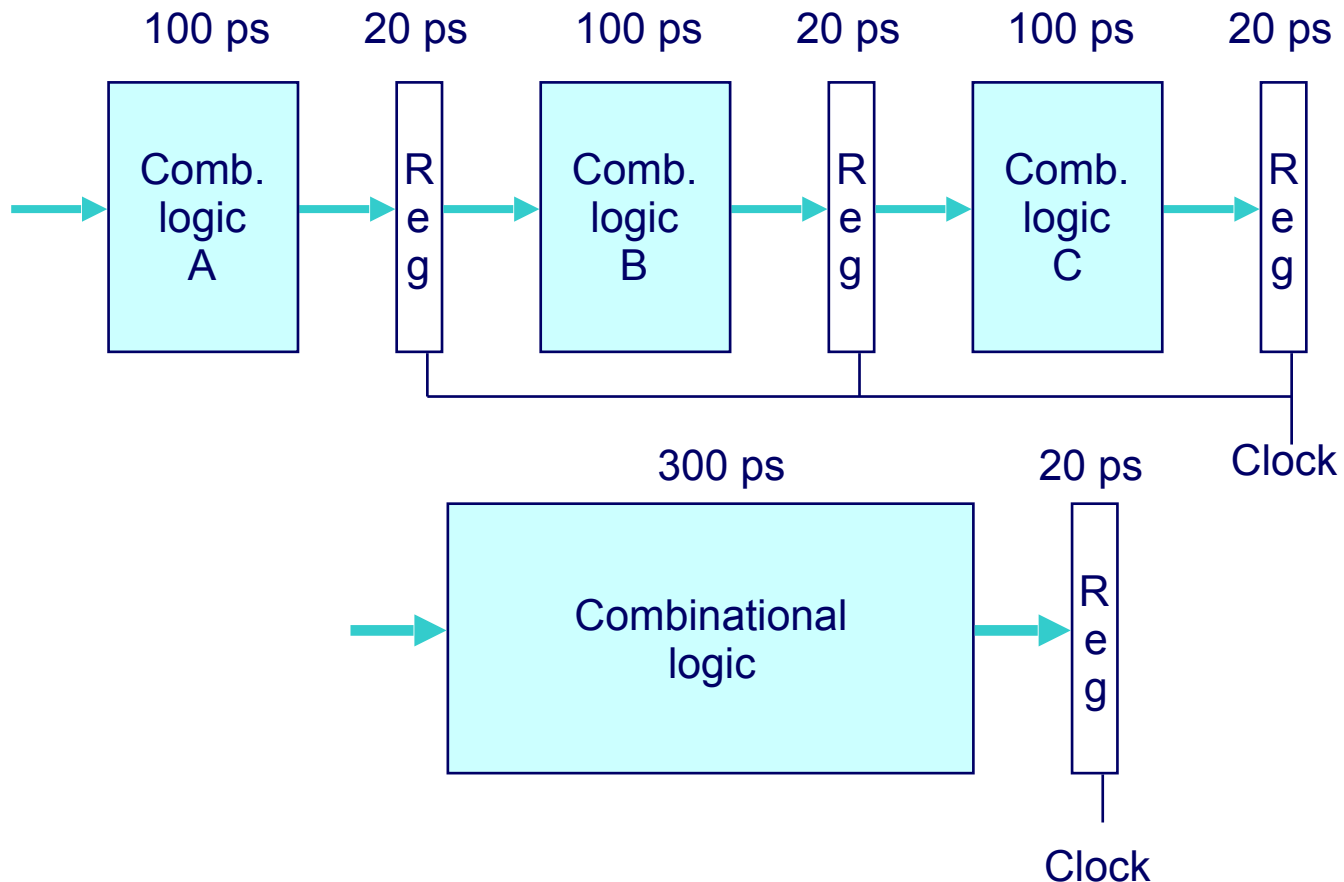
A3 due Thursday, let us know about partners and/or slip days before the due date!

Midterm in one week, counts for 25% of final grade

- Material from today may be included on the exam
- Some review today
- Even more review next class
- 15% partial credit for “I don’t know”, but must erase or cross out anything else on that question

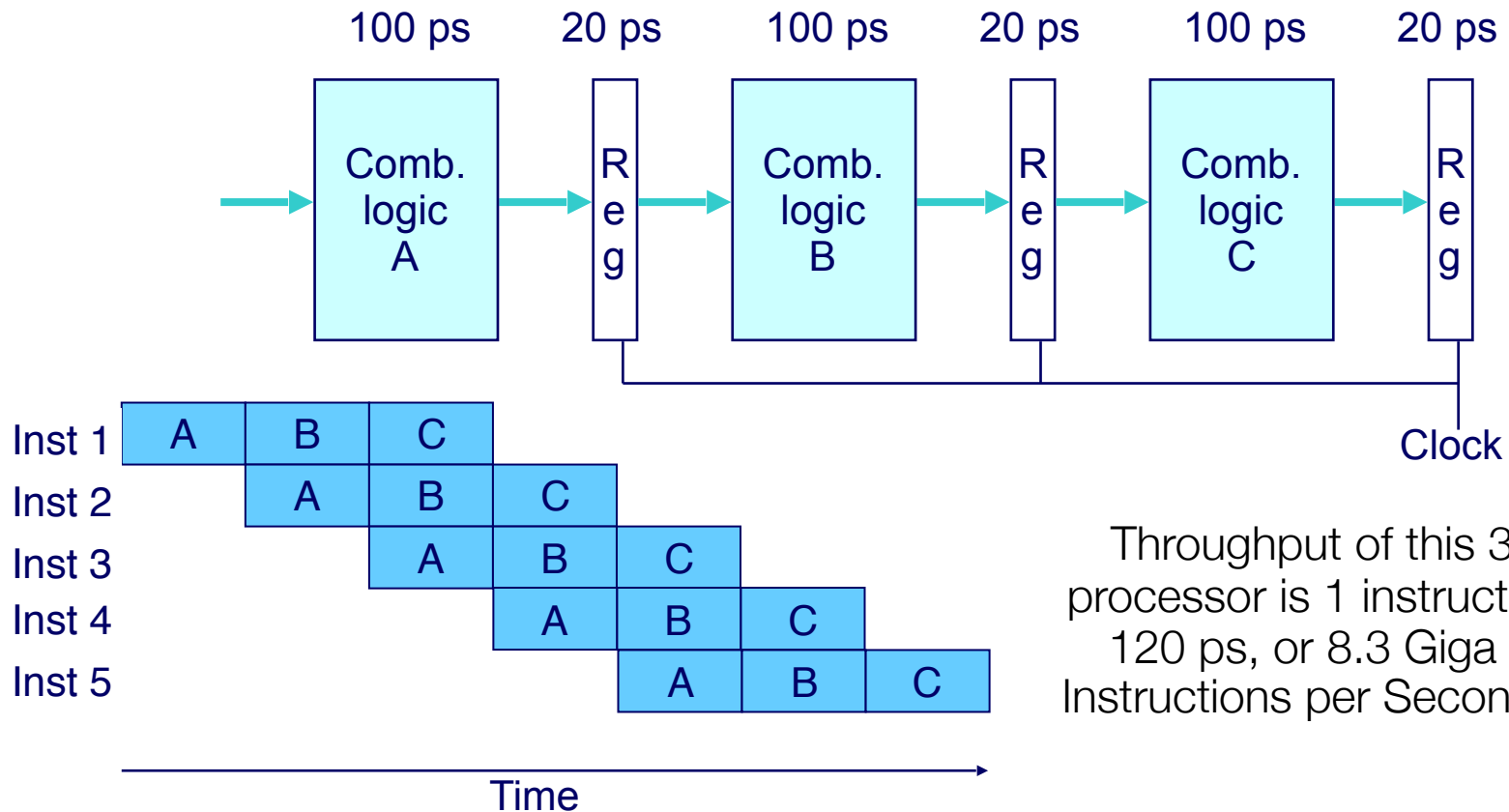
# Pipeline Trade-offs

- Pros: Decrease the total execution time (Increase the “**throughput**”).
- Cons: Increase the latency of each instruction as new registers are needed between pipeline stages.



# Throughput

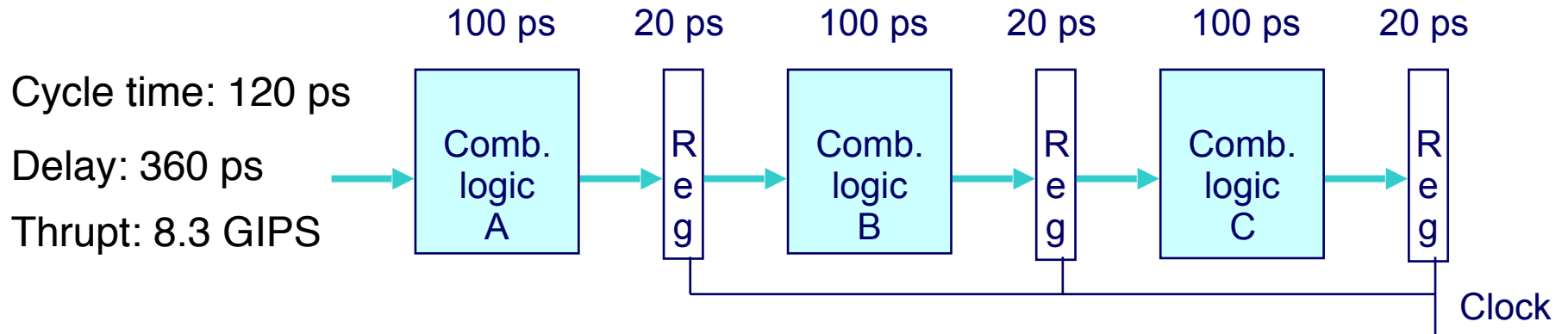
- The rate at which the processor can finish executing an instruction (at the steady state).



Throughput of this 3-stage processor is 1 instruction every 120 ps, or 8.3 Giga (billion) Instructions per Second (GIPS).

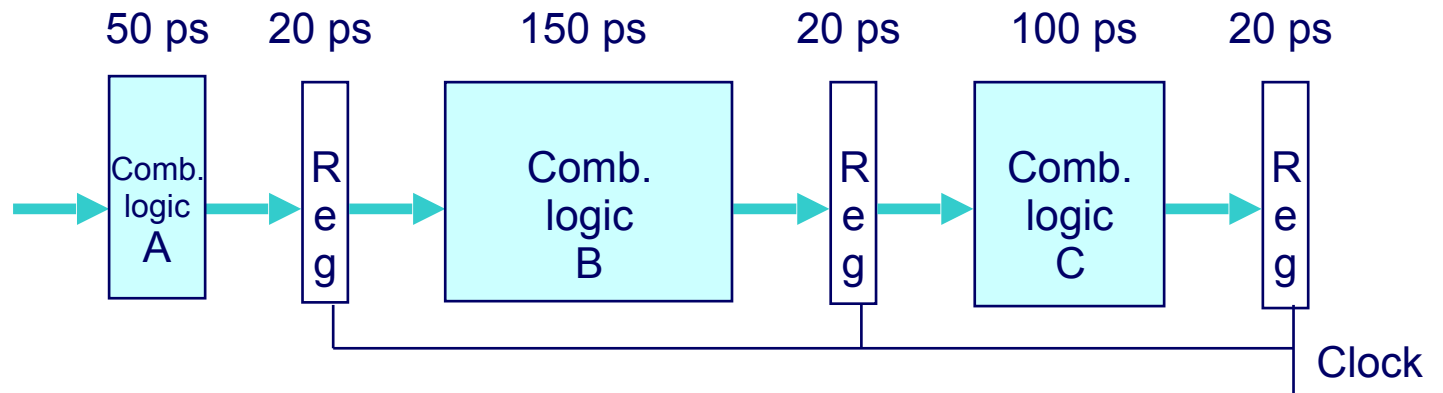
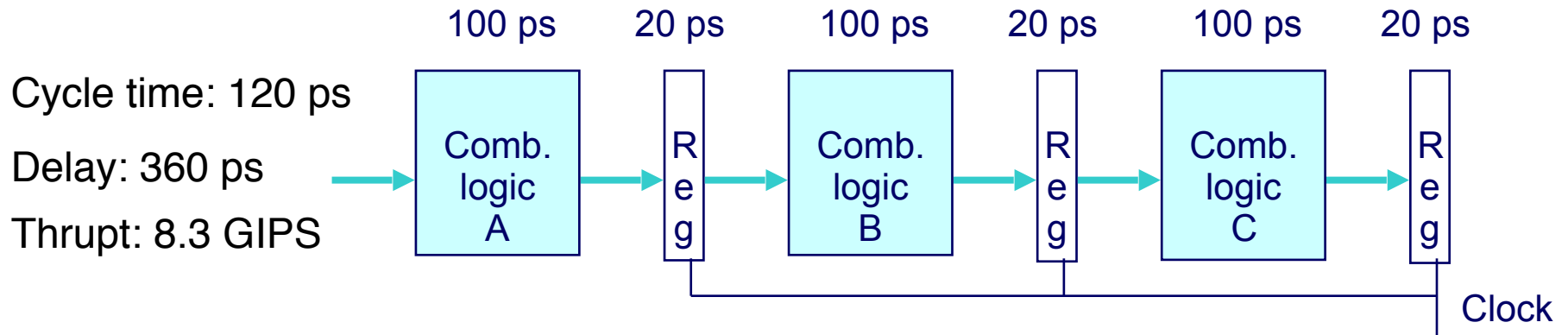
# Aside: Unbalanced Pipeline

- A pipeline's delay is limited by the slowest stage. This limits the cycle time and the throughput



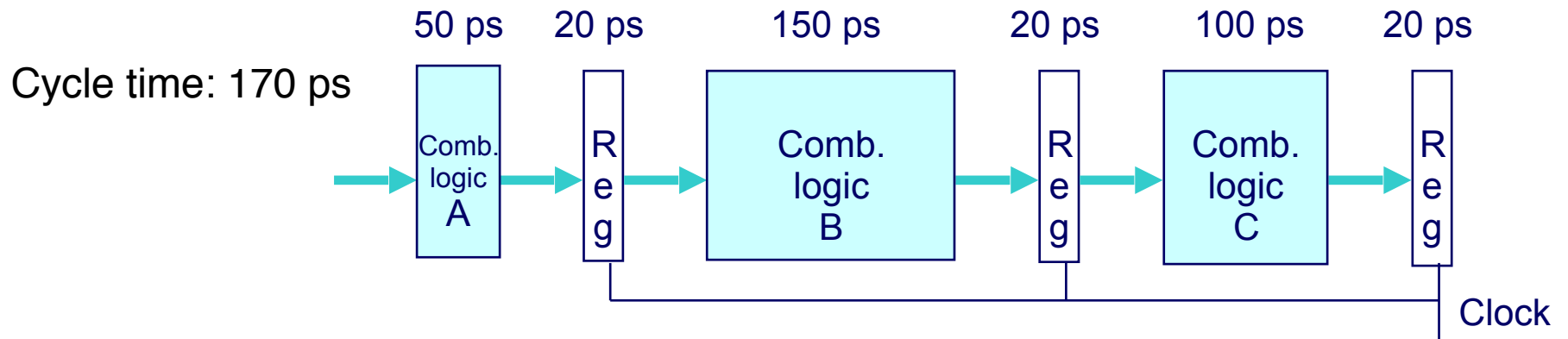
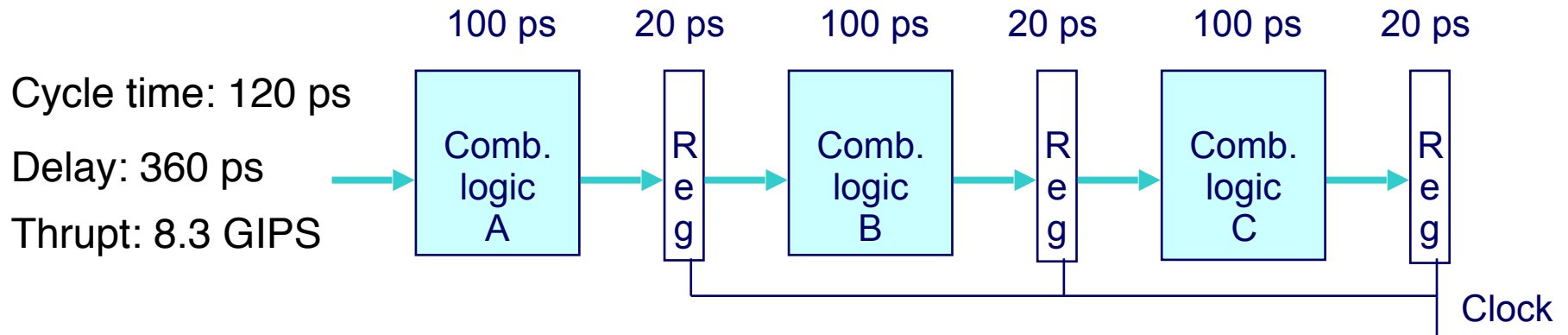
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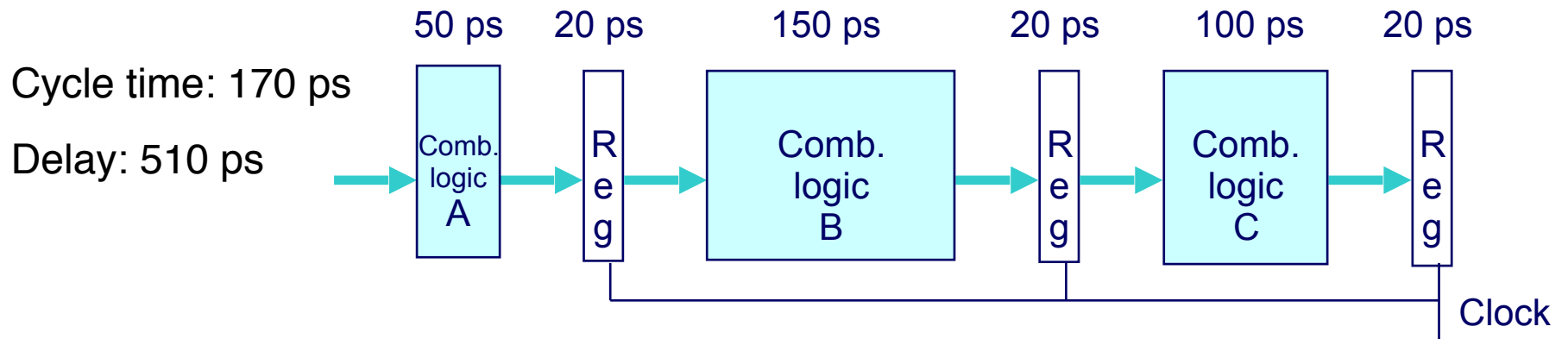
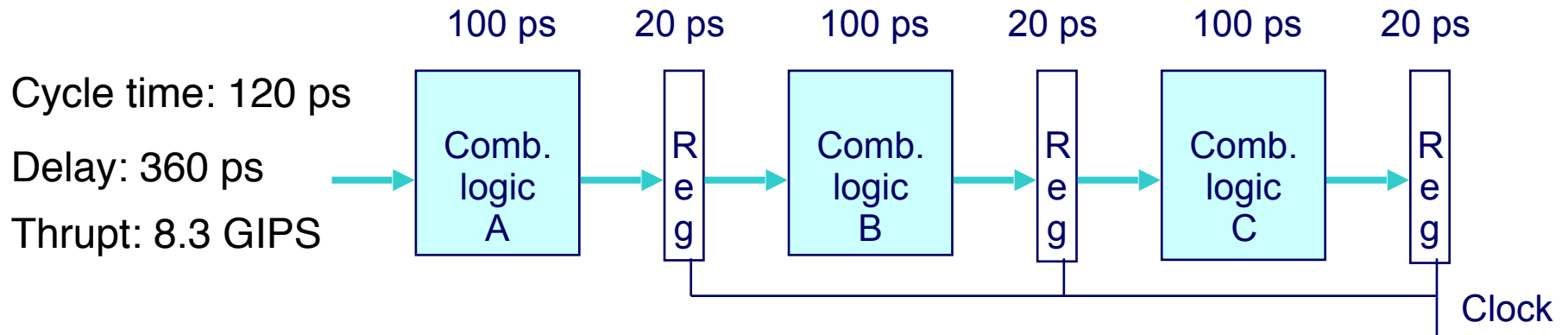
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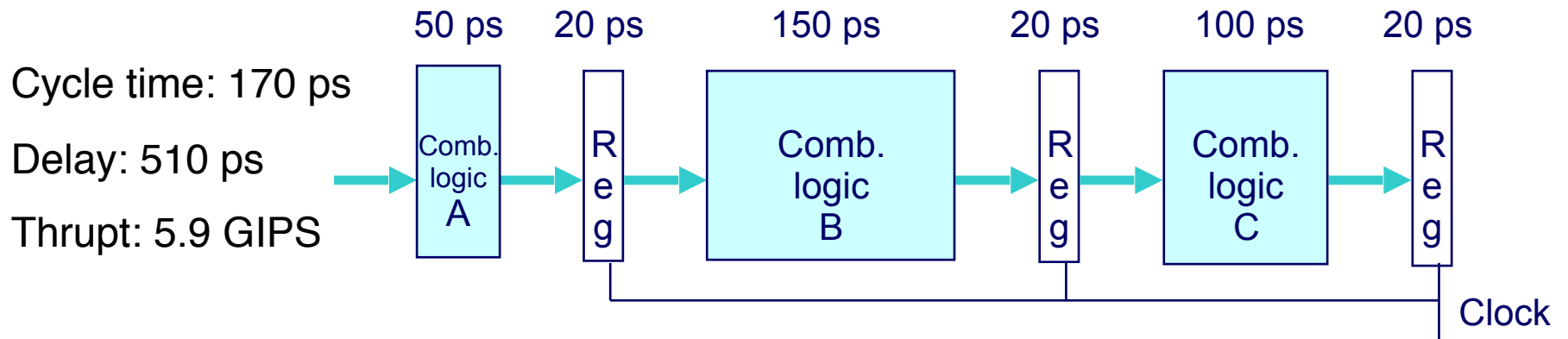
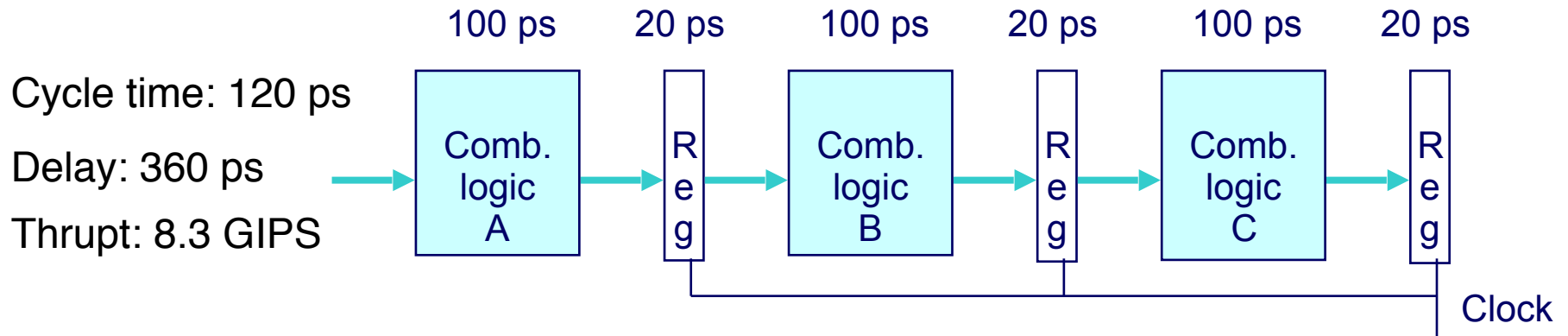
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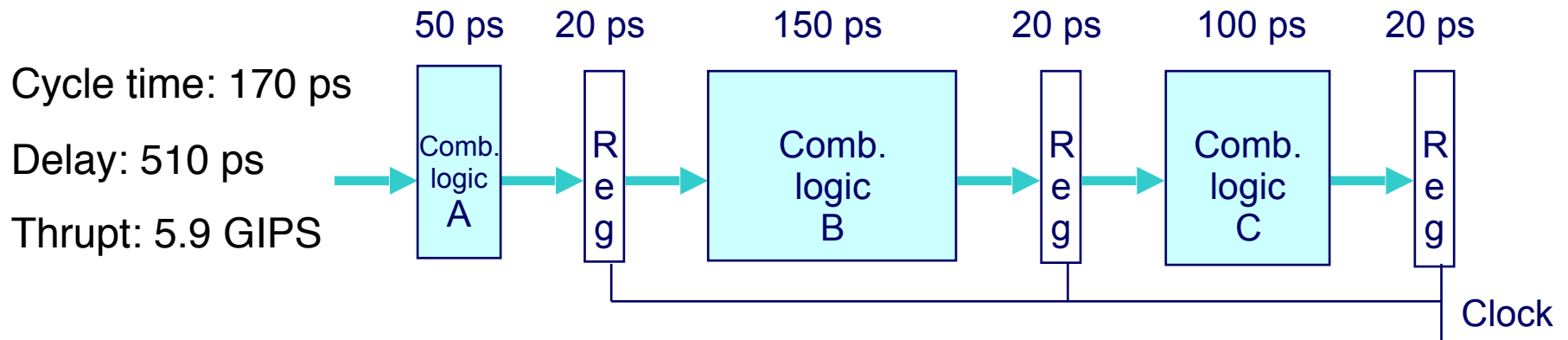
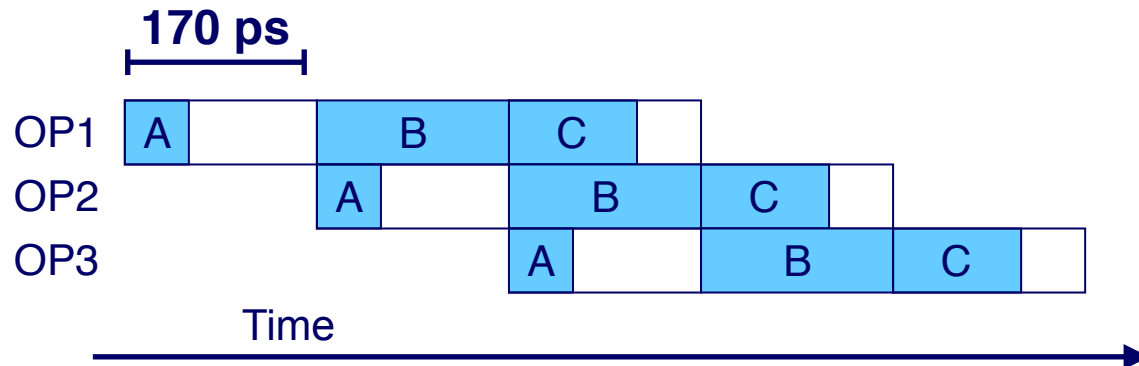
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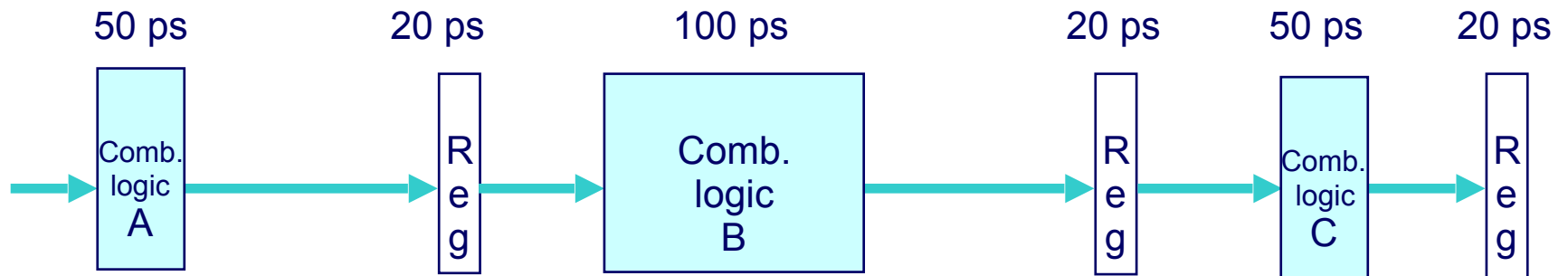
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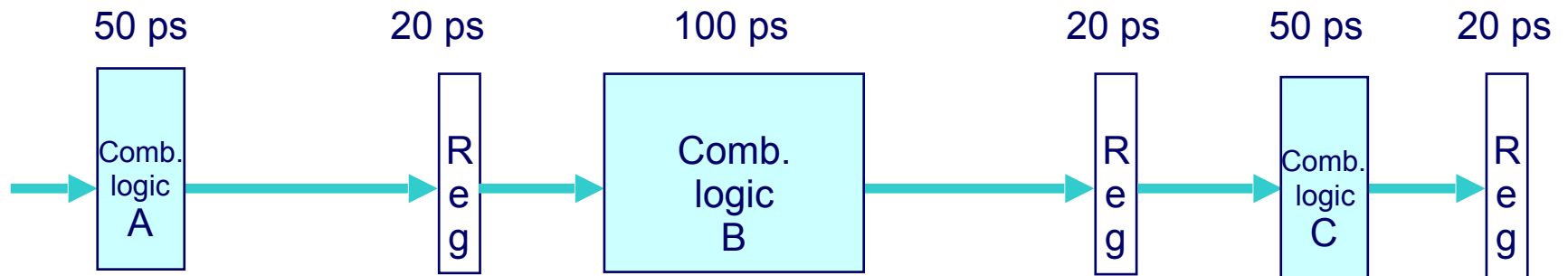
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- Solution 1: Further pipeline the slow stages



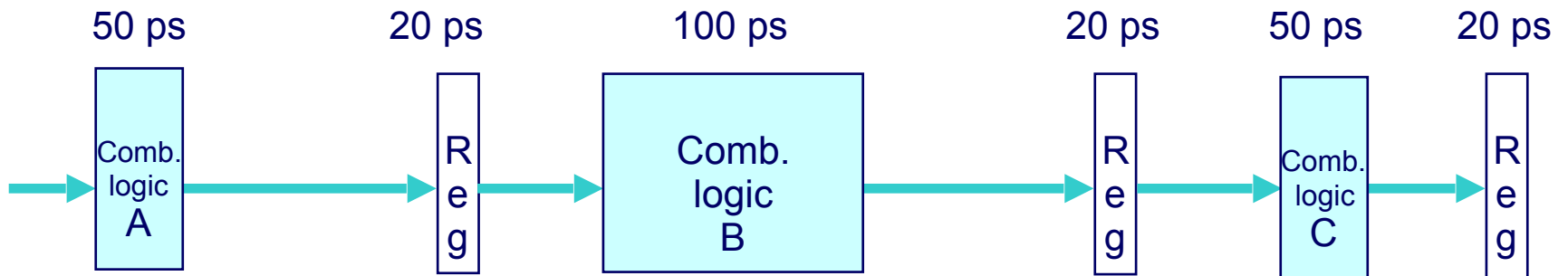
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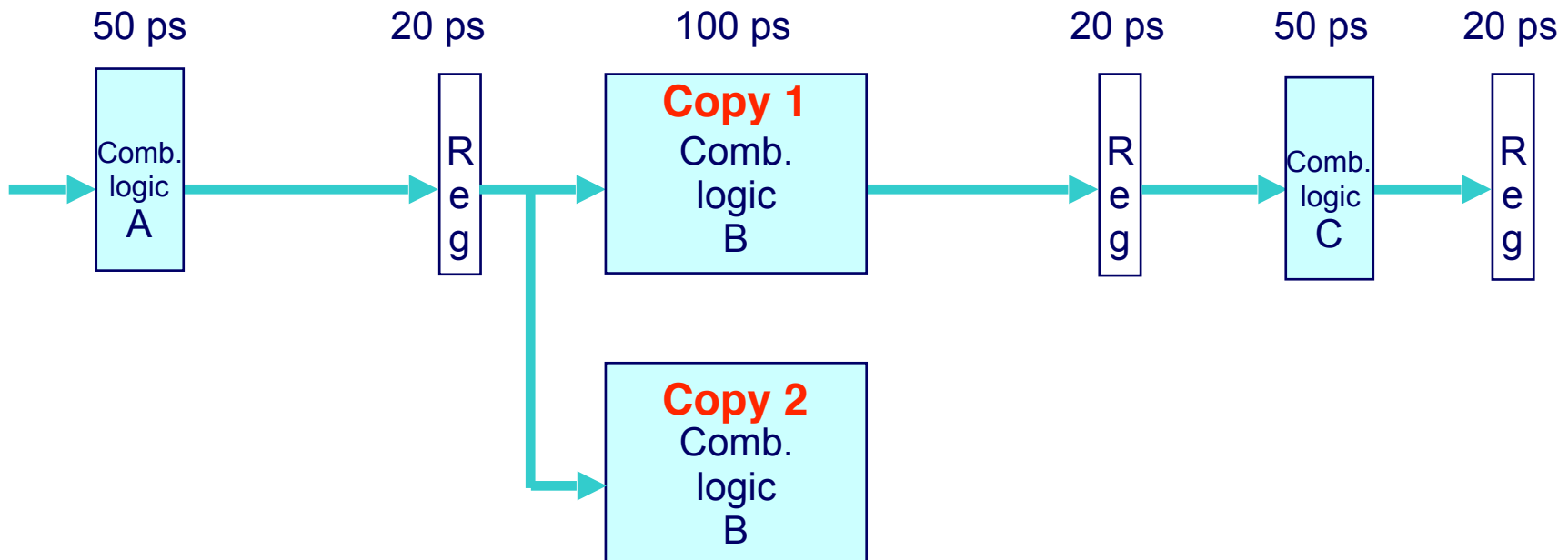
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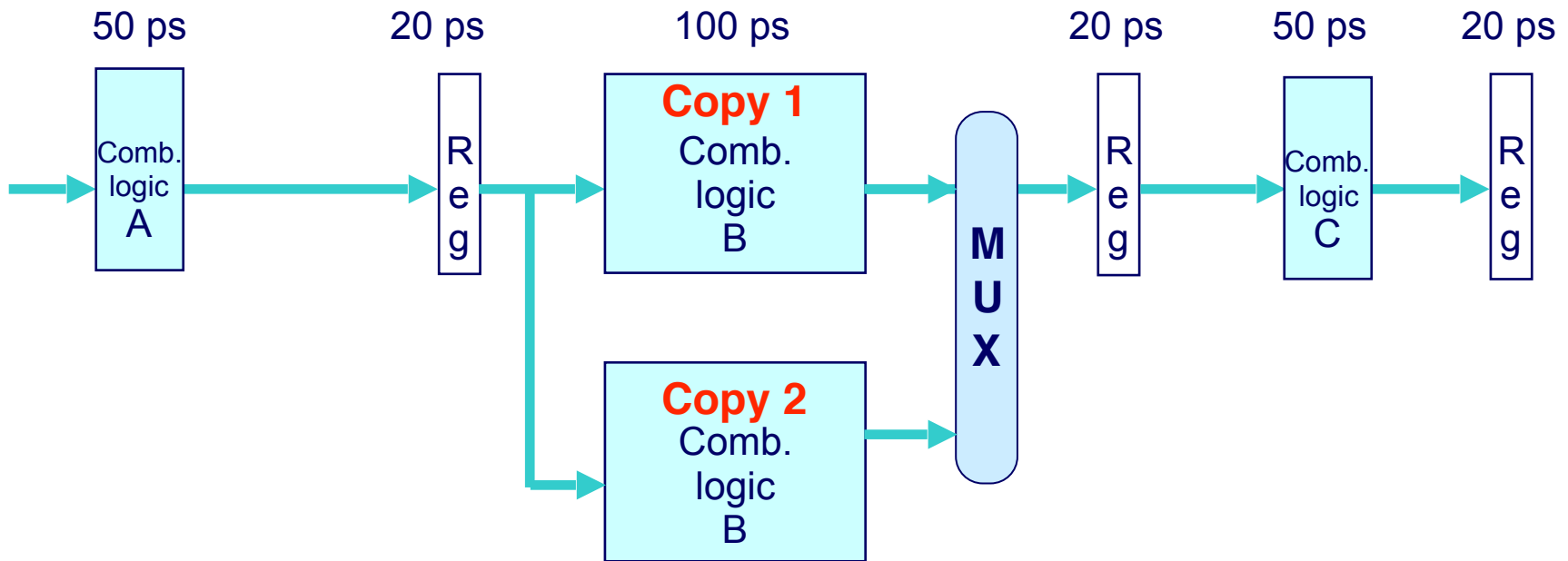
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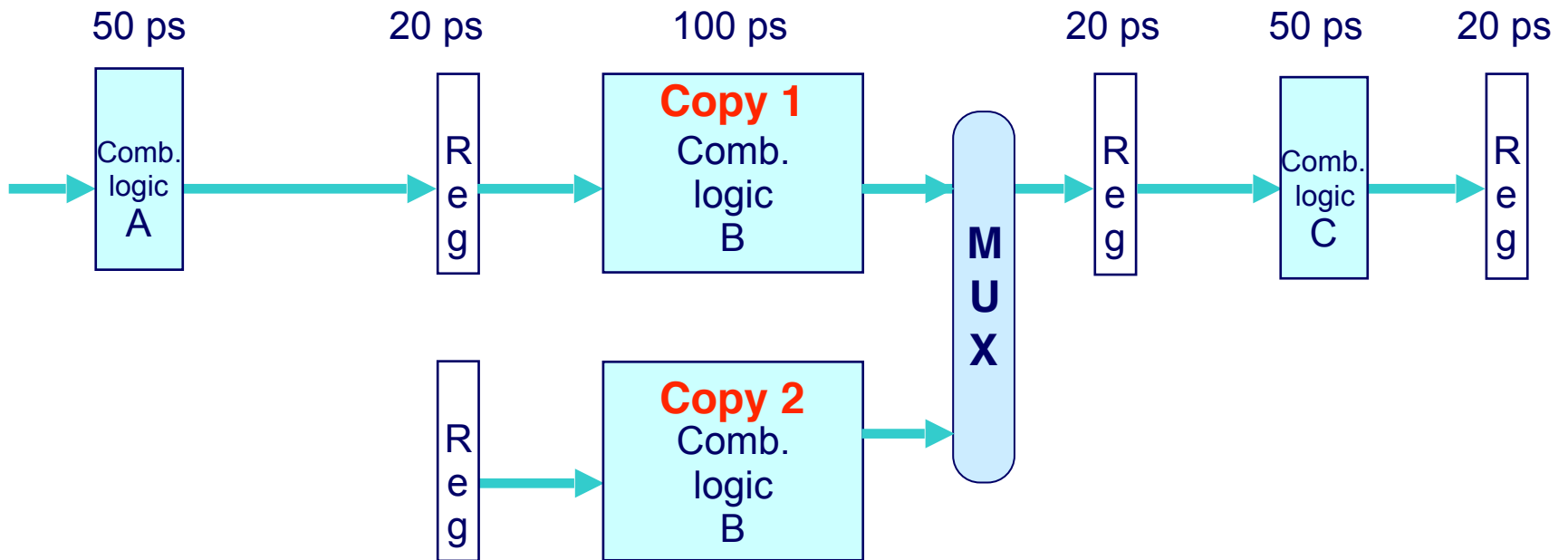
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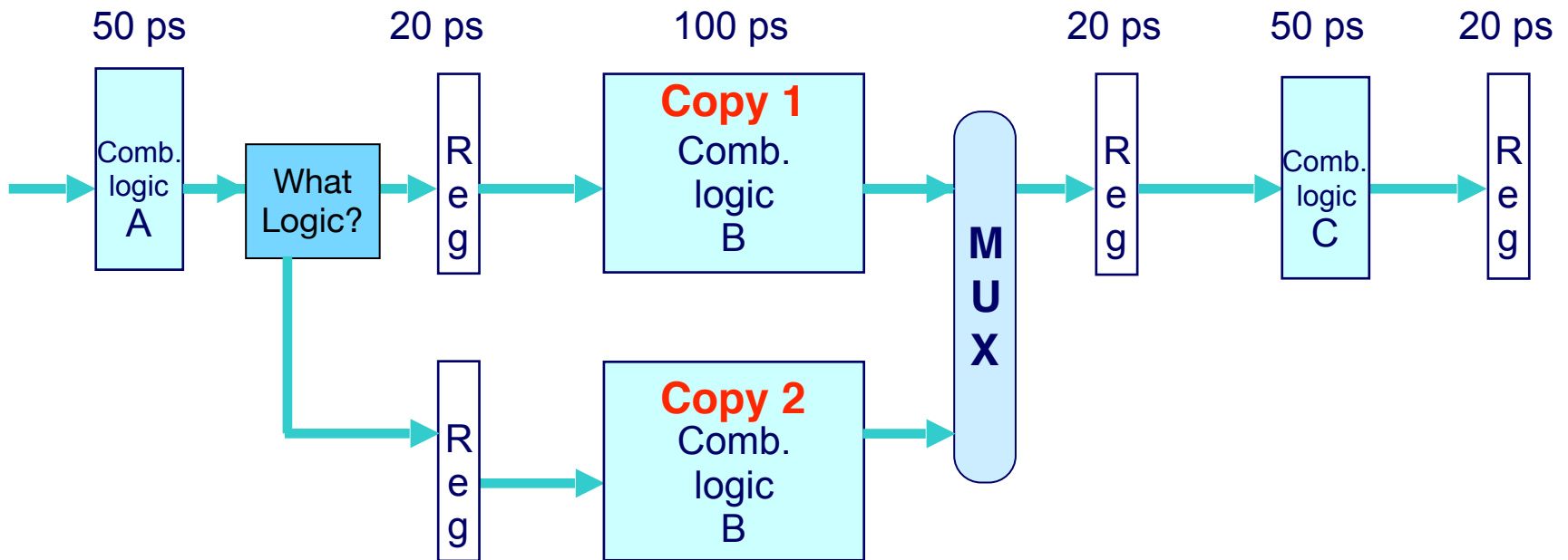
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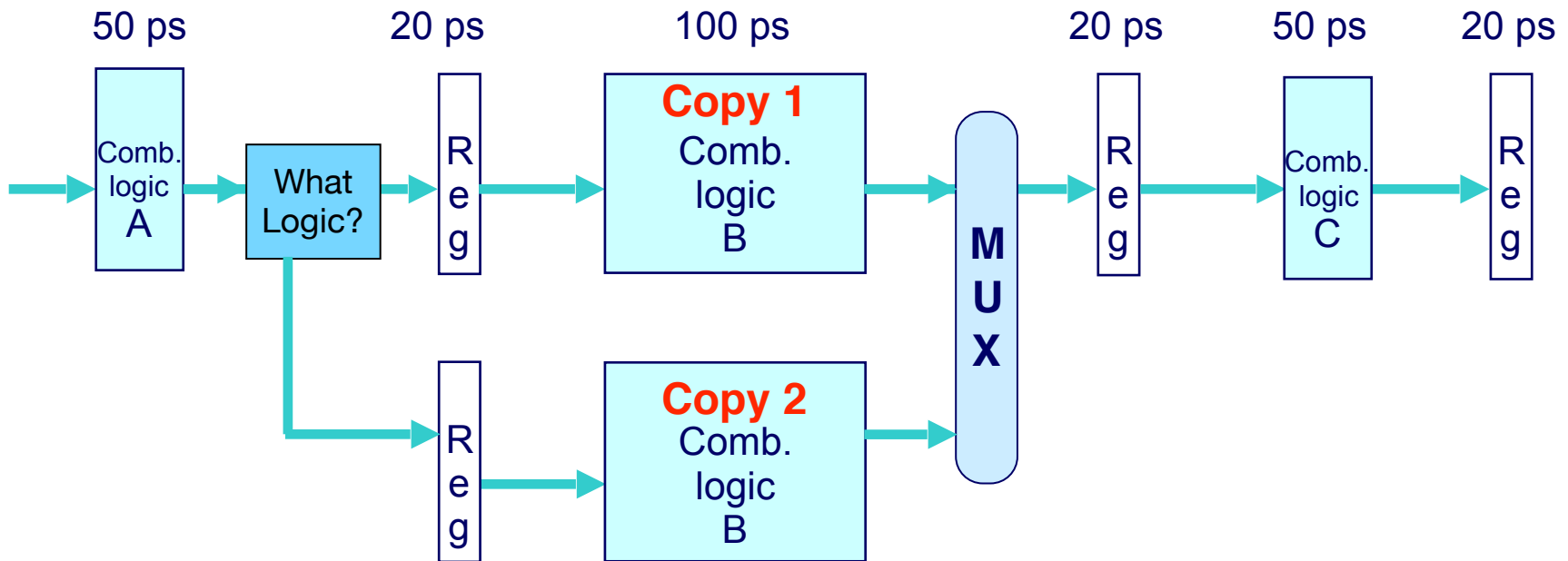
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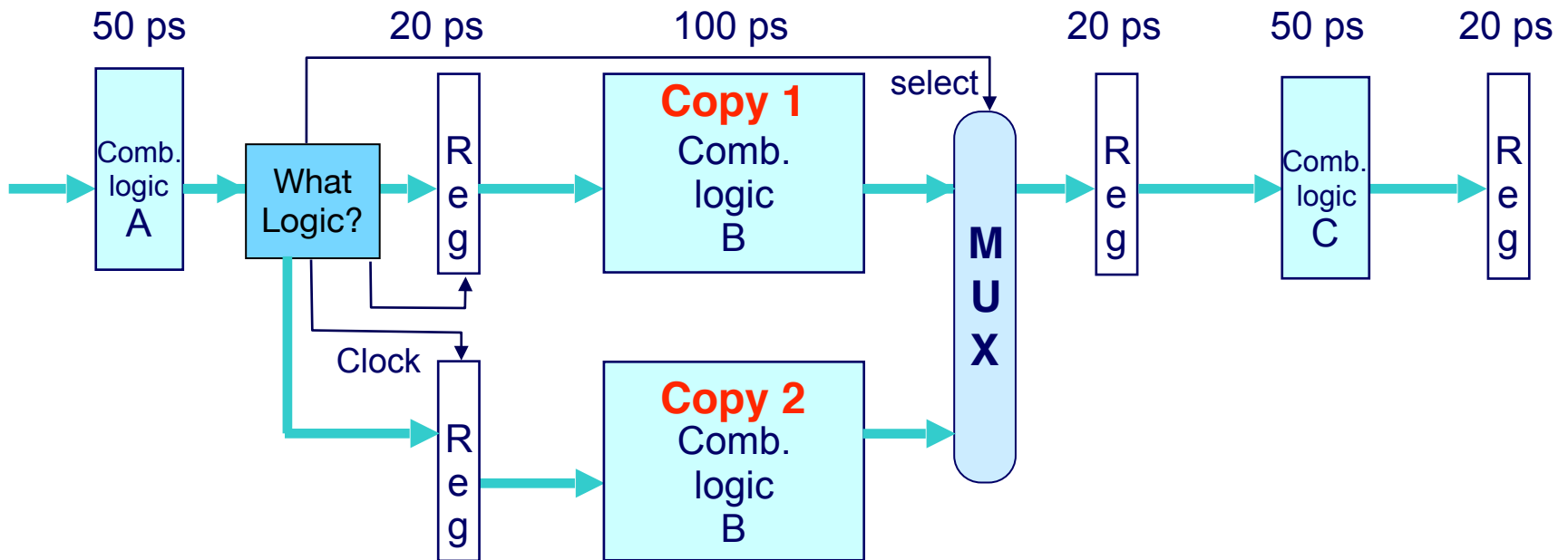


What logic do you need there?

Hint: it needs to control the clock signals of the two registers and the select signal of the MUX.

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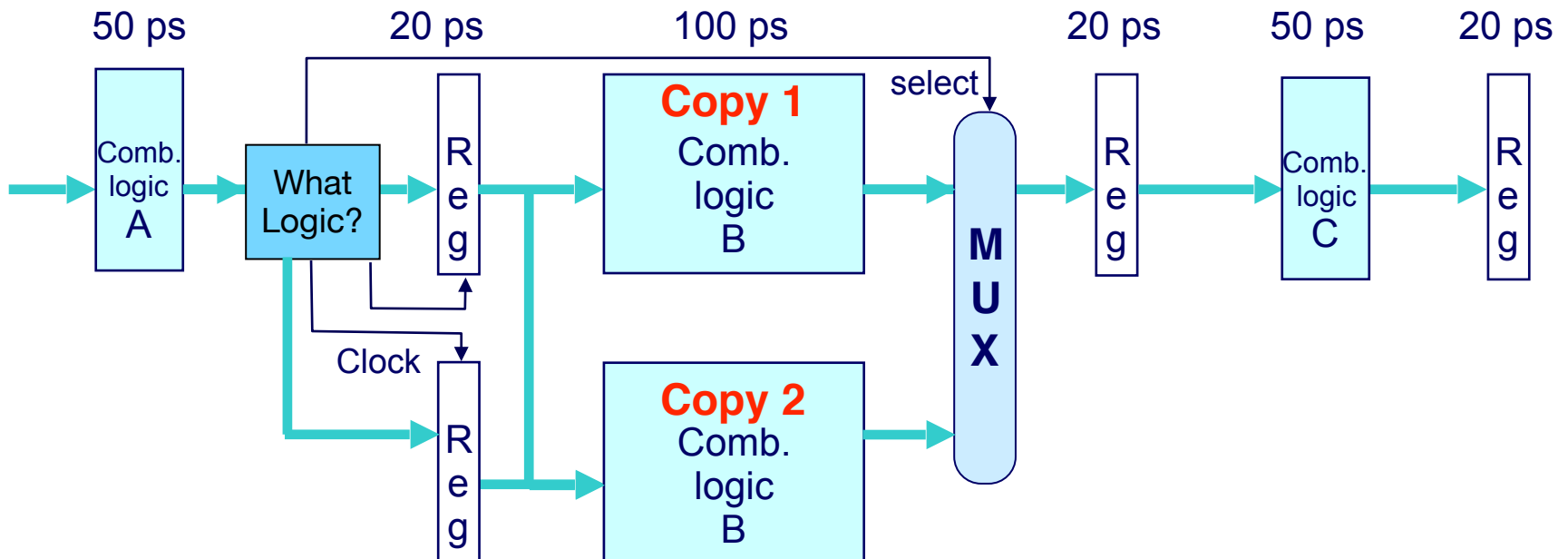


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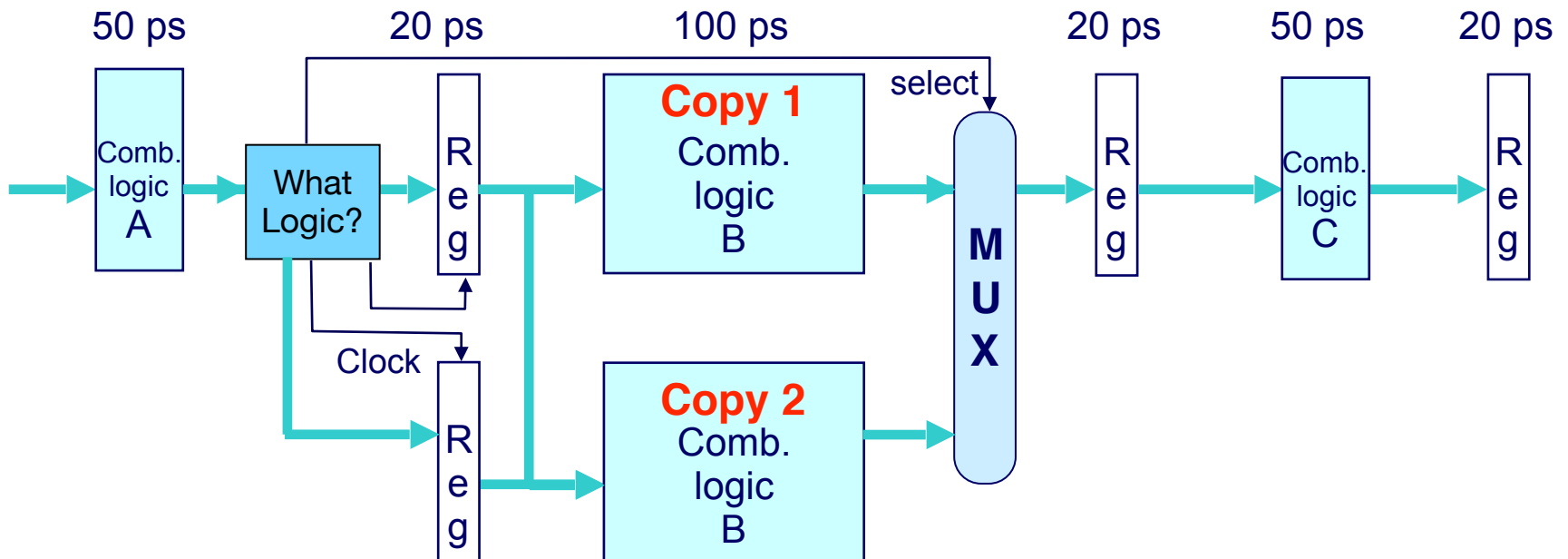
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- Data sent to copy 1 in odd cycles and to copy 2 in even cycles.



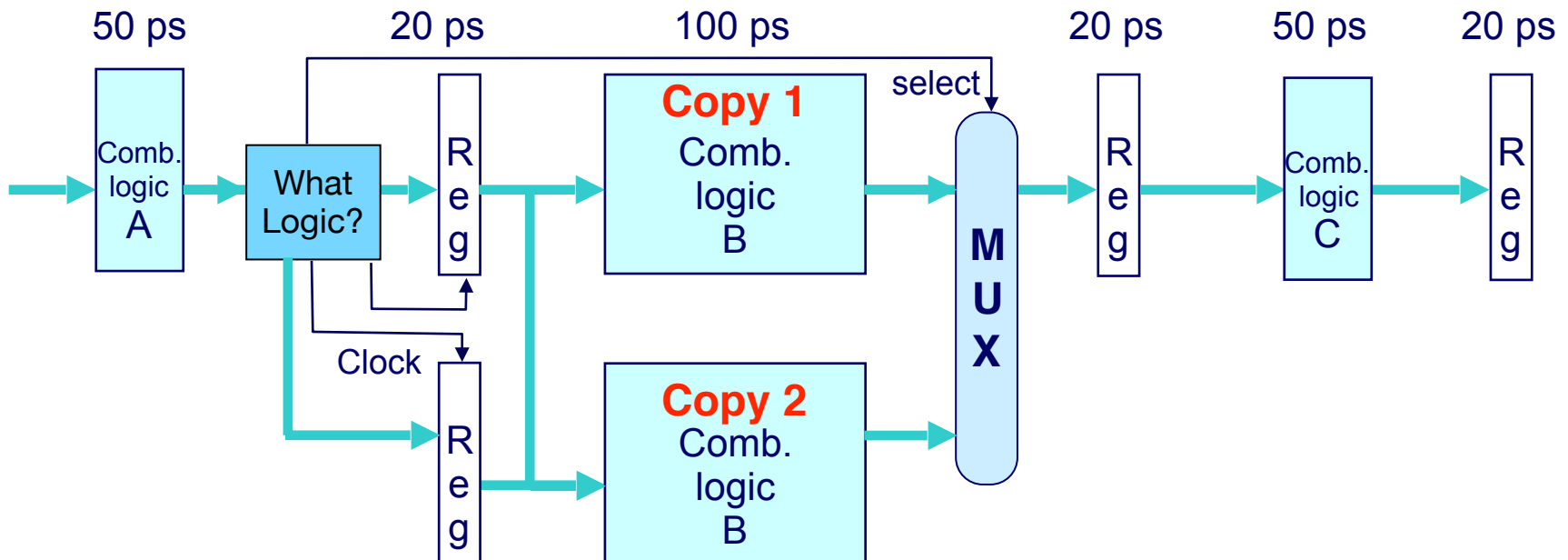
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- Data sent to copy 1 in odd cycles and to copy 2 in even cycles.
- This is called 2-way interleaving. Effectively the same as pipelining Comb. logic B into two sub-stages.
- The cycle time is reduced to 70 ps (as opposed to 120 ps) at the cost of extra hardware.



# Pipeline Stages

## Fetch

- Use PC to read instruction
- **Compute new PC for non-jump instructions**

## Decode

- Read program registers

## Execute

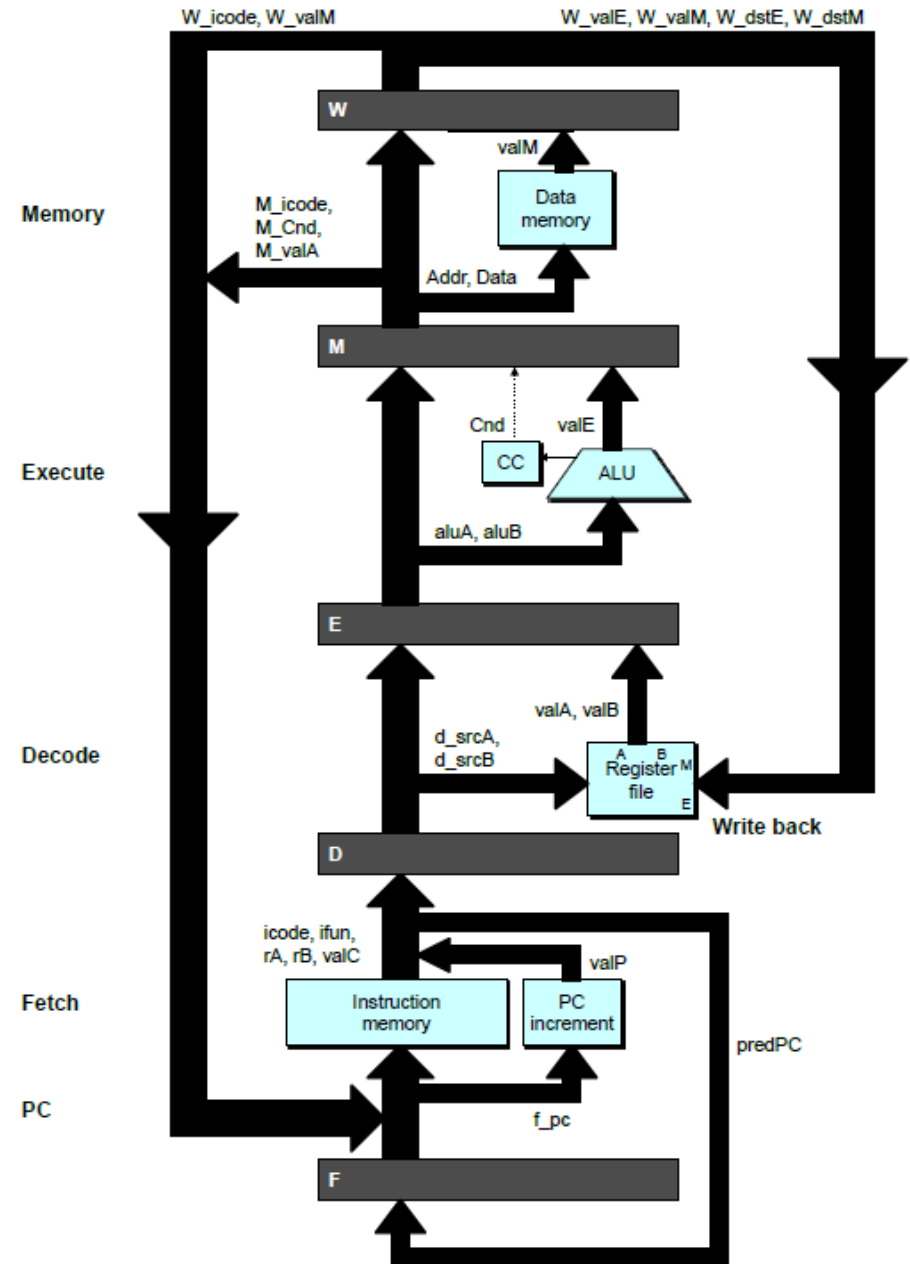
- Operate ALU
- **Compute new PC for jump instructions**

## Memory

- Read or write data memory

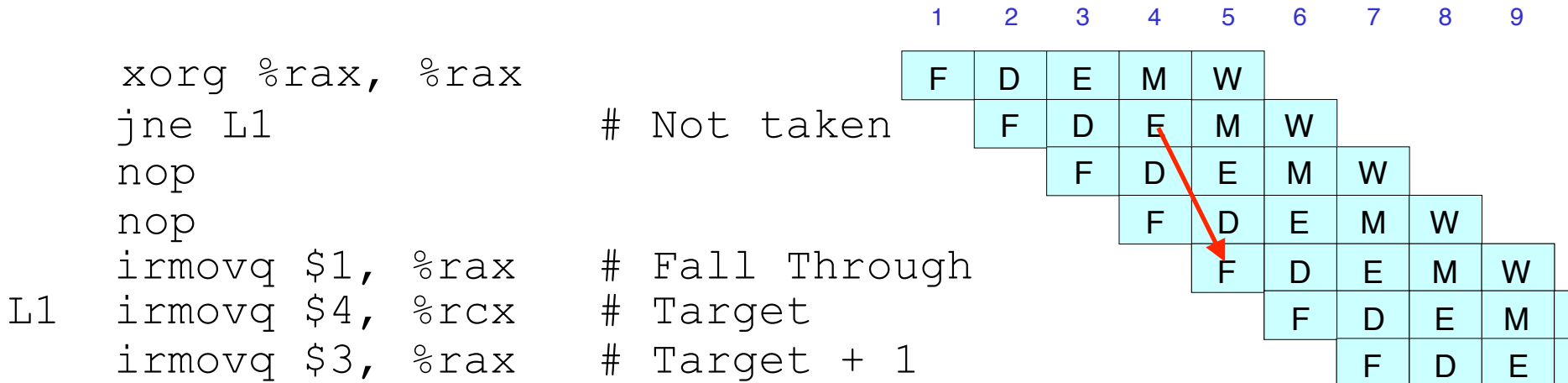
## Write Back

- Update register file



# Control Dependency

- **Definition:** Outcome of instruction A determines whether or not instruction B should be executed or not.
- Jump instruction example below:
  - `jne L1` determines whether `irmovq $1, %rax` should be executed
  - But `jne` doesn't know its outcome until after its Execute stage





# Better Pipelining

## Fetch

- Use PC to read instruction
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## Execute

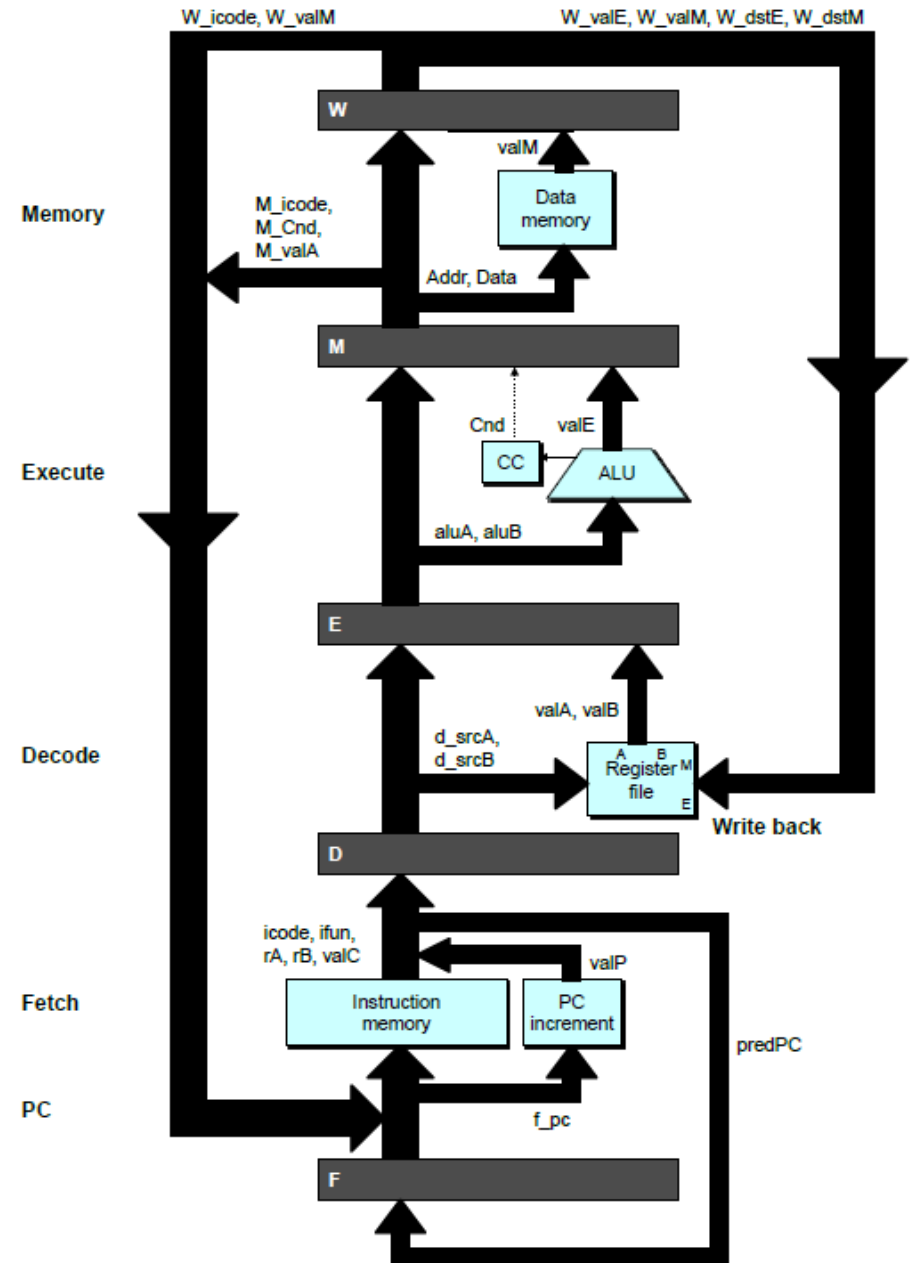
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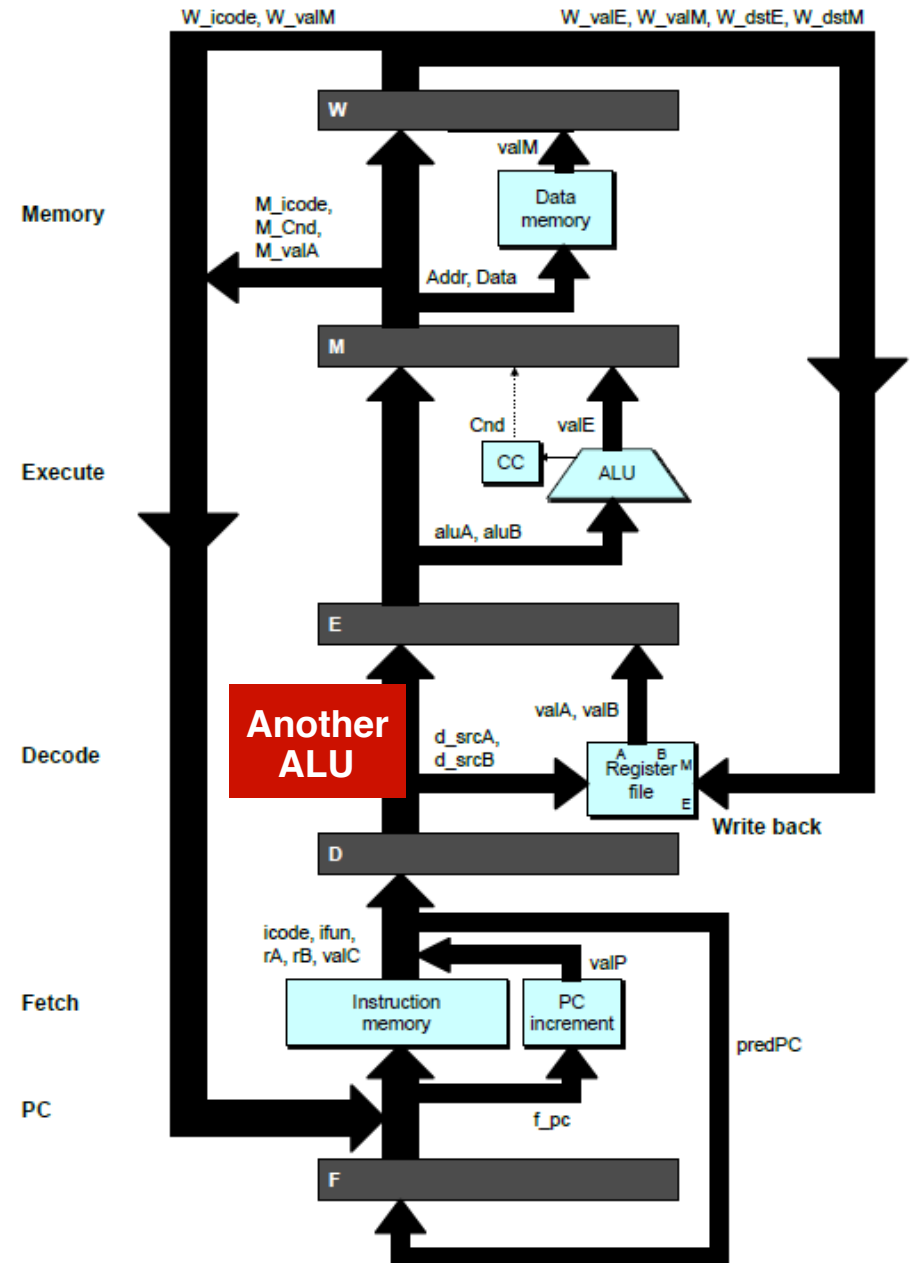
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# Resolving Control Dependencies

- **Software Mechanisms**

- Adding NOPs: requires compiler to insert nops, which also take memory space — not a good idea
- Delay slot: insert instructions that do not depend on the effect of the preceding instruction. These instructions will execute even if the preceding branch is taken — old RISC approach

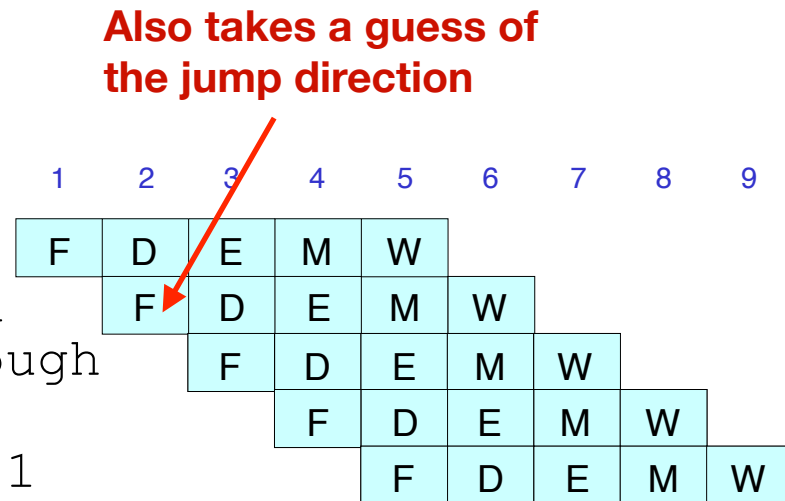
- **Hardware mechanisms**

- Stalling (Think of it as hardware automatically inserting nops)
- Branch Prediction
- Return Address Stack

# Branch Prediction

Idea: instead of waiting, why not just guess the direction of jump?

```
xorg %rax, %rax
jne L1 # Not taken
irmovq $1, %rax # Fall Through
L1: irmovq $4, %rcx # Target
    irmovq $3, %rax # Target + 1
```

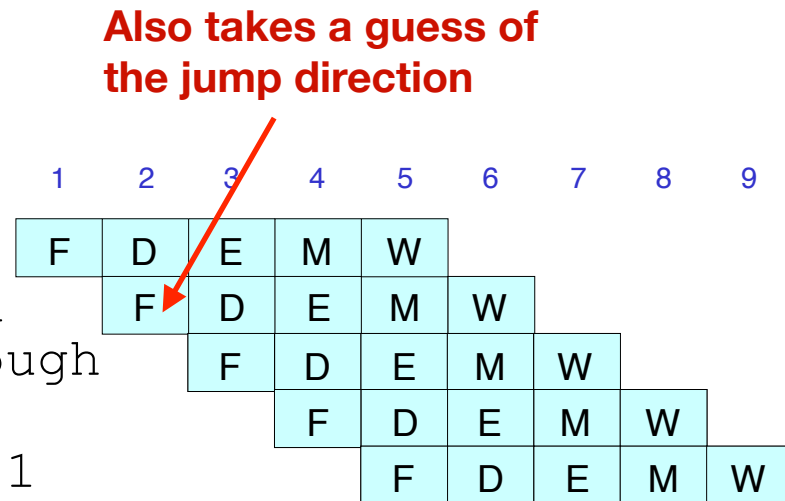


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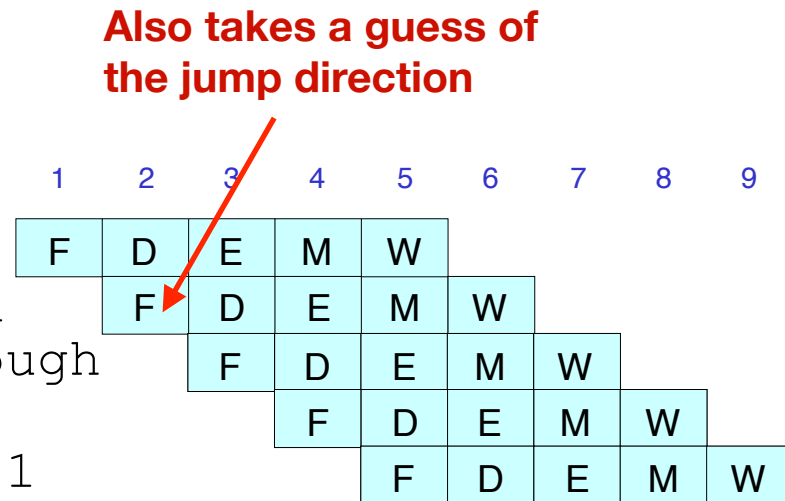
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## Static Prediction

- Always Taken
- Always Not-taken

## Dynamic Prediction

- Dynamically predict taken/not-taken for each specific jump instruction



# Static Prediction

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Observation (Assumption really): Two uses of jumps

- People use jumps to check corner cases. These branches are mostly not taken because corner cases are rare.
- People use jumps to implement loops. These branches are mostly taken because a loop takes multiple iterations.

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    cmpq    %rsi,%rdi
    jle    .corner_case
    <do_A>
.corner_case:
    <do_B>
    ret
```

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```
    cmpq    %rsi, %rdi           <before>
    jle    .corner_case        .L1: <body>
    <do_A>
.corner_case:
    <do_B>           Mostly not taken
    ret
    cmpq    B, A
    jl     .L1
    <after>
```




# Static Prediction

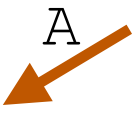
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## Strategy:

- Forward jumps (i.e., `if-else`): always predict not-taken
- Backward jumps (i.e., `loop`): always predict taken

```
cmpq    %rsi, %rdi    <before>
jle     .corner_case  .L1: <body>
<do_A>
        .corner_case:  <do_B>
        <do_B>
        ret            <after>
```

**Mostly not taken** (arrow pointing to `.corner_case`)

**Mostly taken** (arrow pointing to `jle .L1`)

# Static Prediction

Knowing branch prediction strategy helps us write faster code

- Any difference between the following two code snippets?
- What if you know that hardware uses the always non-taken branch prediction?

```
if (cond) {  
    do_A()  
} else {  
    do_B()  
}
```

```
if (!cond) {  
    do_B()  
} else {  
    do_A()  
}
```



# Dynamic Prediction

- Simplest idea:
  - If last time taken, predict taken; if last time not-taken, predict not-taken
  - Called 1-bit branch predictor
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Iteration #1	0	1	2	3	4
Predicted Outcome	<b>N</b>	T	T	T	<b>T</b>
Actual Outcome	T	T	T	T	N

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Predict with 1-bit	<b>N</b>	T	T	T	<b>T</b>
Actual Outcome	T	T	T	T	N
Predict with 2-bit	<b>N</b>	<b>N</b>	T	T	<b>T</b>

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Predict with 1-bit	<b>N</b>	T	T	T	<b>T</b>	<b>N</b>	T	T	T	<b>T</b>
Actual Outcome	T	T	T	T	N	T	T	T	T	N
Predict with 2-bit	<b>N</b>	<b>N</b>	T	T	<b>T</b>	T	T	T	T	<b>T</b>

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Actual Outcome	T	T	T	T	N	T	T	T	T	N	T	T	T	T	N
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Predict with 2-bit	N	N	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T

# More Advanced Dynamic Prediction

- Look for past histories *across instructions*
- Branches are often correlated
  - Direction of one branch determines another

cond1 branch not-  
taken means  $(x \leq 0)$   
branch taken

```
x = 0
if (cond1) x = 3
if (cond2) y = 19
if (x <= 0) z = 13
```



# Today: Making the Pipeline Really Work


- Control Dependencies
  - Inserting Nops
  - Stalling
  - Delay Slots
  - Branch Prediction
- Data Dependencies
  - Inserting Nops
  - Stalling
  - Out-of-order execution

# Data Dependencies

```
1    irmovq $50, %rax
2    addq   %rax, %rbx
3    mrmovq 100(%rbx), %rdx
```

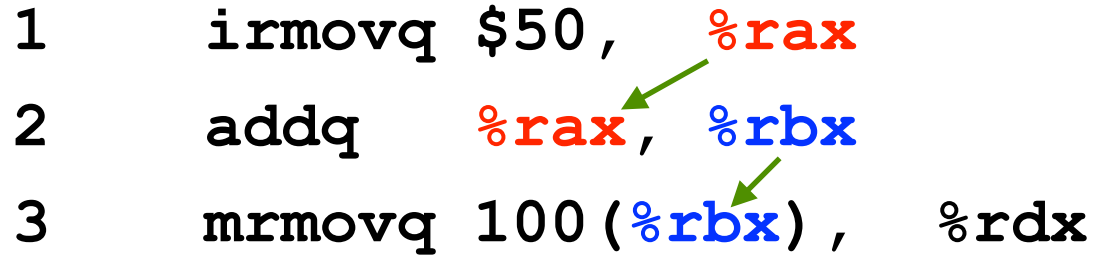
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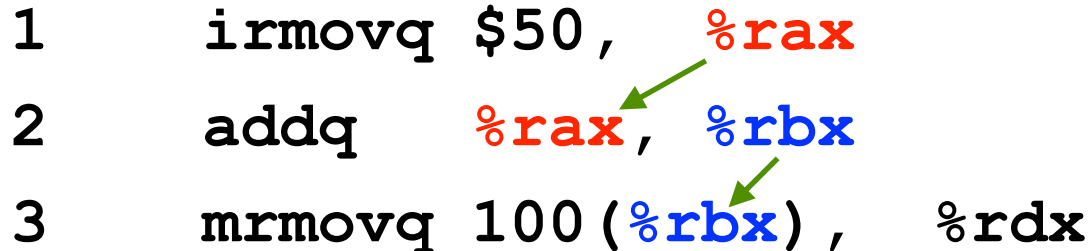
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- Result from one instruction used as operand for another
  - **Read-after-write (RAW)** dependency
- Very common in actual programs
- Must make sure our pipeline handles these properly
  - Get correct results
  - Minimize performance impact



# A Subtle Data Dependency

- Jump instruction example below:
  - `jne L1` determines whether `irmovq $1, %rax` should be executed
  - But `jne` doesn't know its outcome **until after its Execute stage.**

**Why?**

```
xorg %rax, %rax
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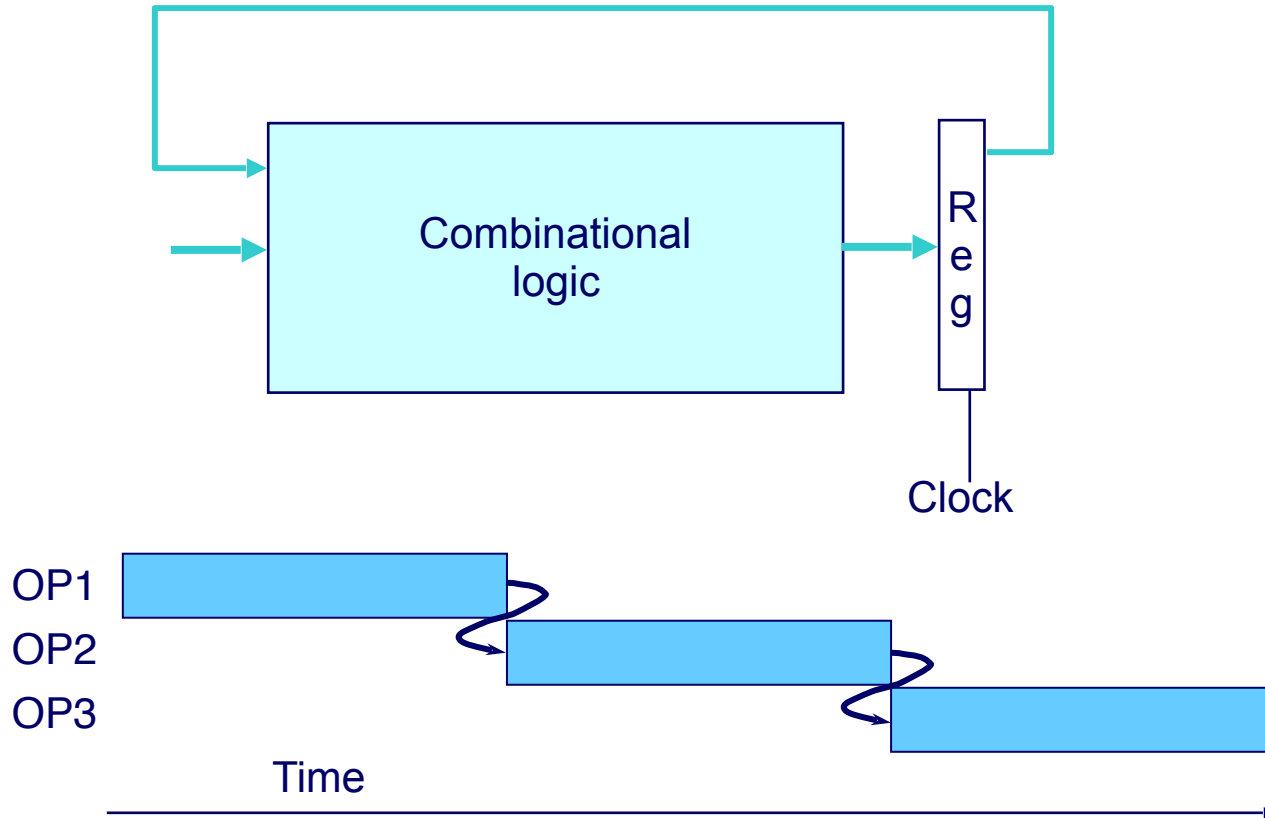
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## Why?

- There is a data dependency between `xorg` and `jne`. The “data” is the status flags.

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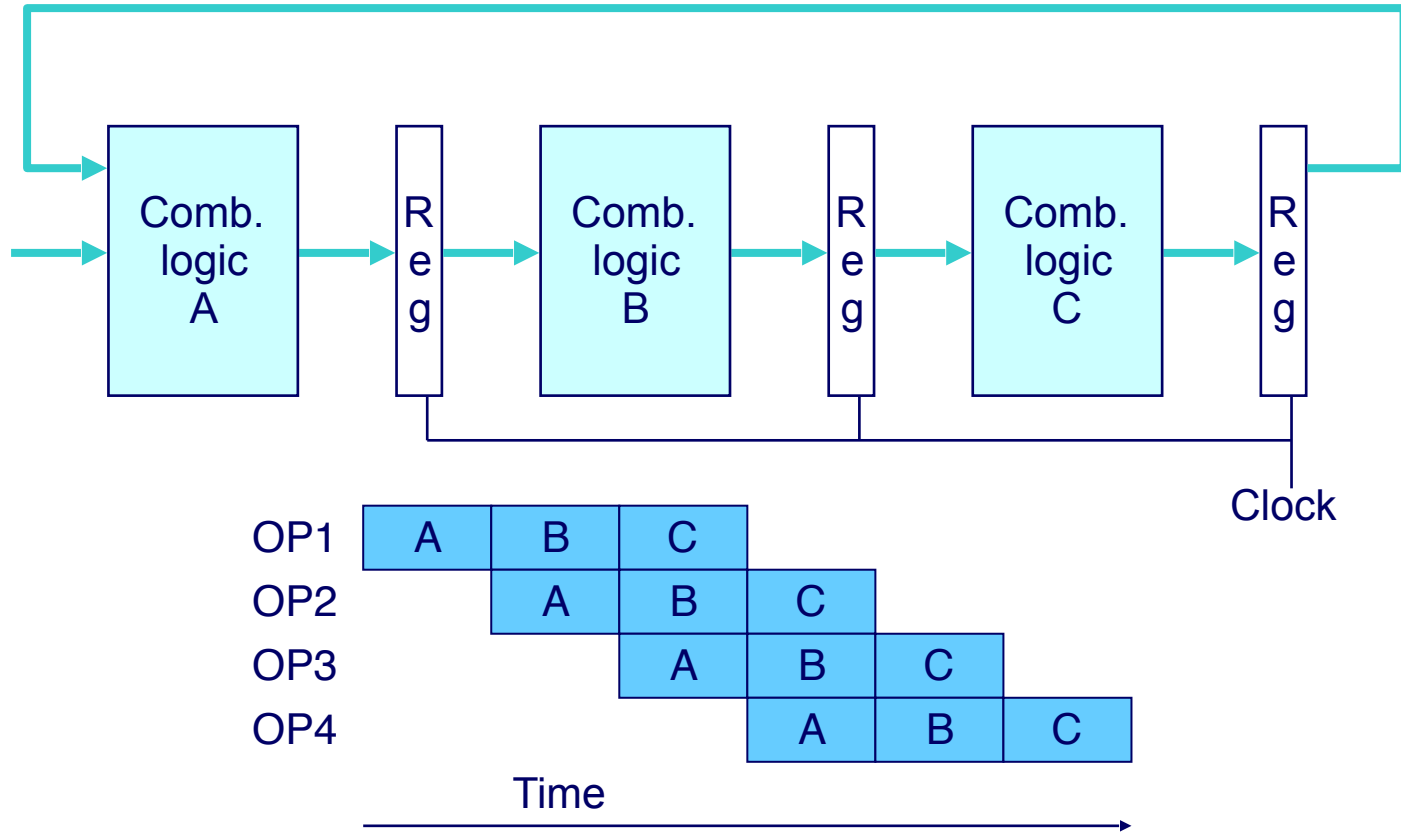
# Data Dependencies in Single-Cycle Machines



## In Single-Cycle Implementation:

- Each operation starts only after the previous operation finishes. Dependency always satisfied.

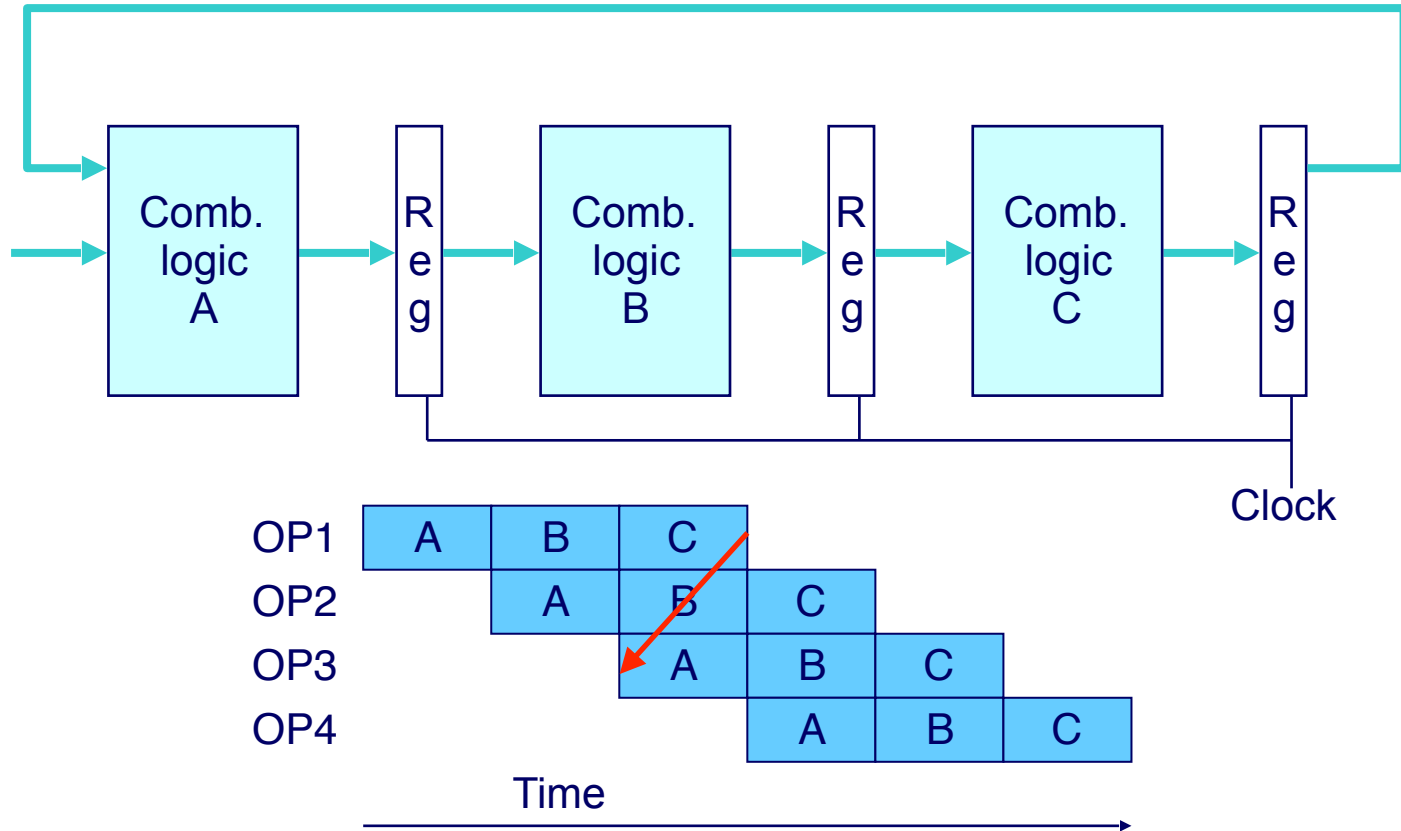
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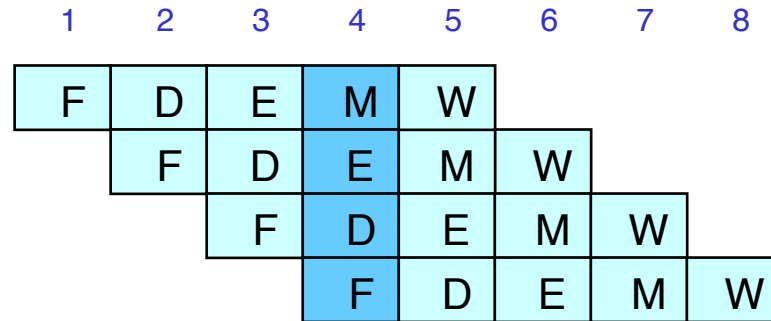
# Data Dependencies: No Nop

0x000: `irmovq $10,%rdx`

0x00a: `irmovq $3,%rax`

0x014: `addq %rdx,%rax`

0x016: `halt`



Remember registers get updated in the Write-back stage

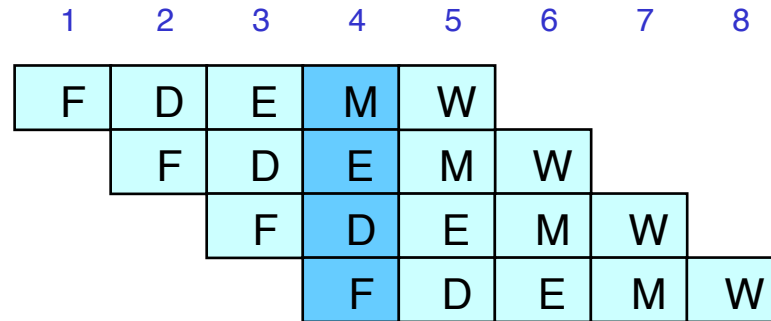
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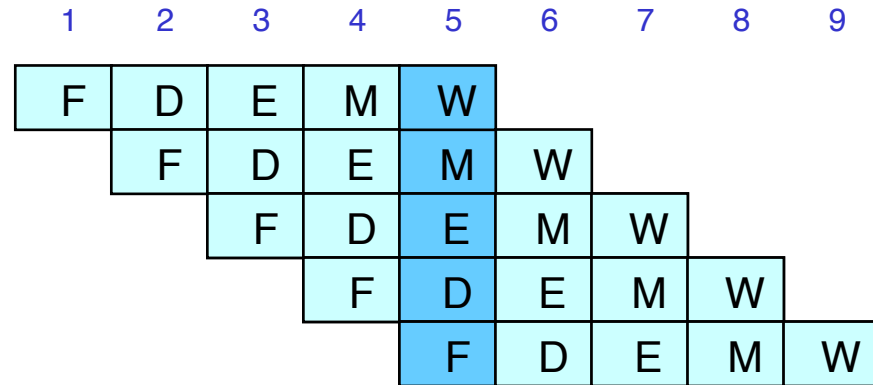


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**addq reads wrong %rdx and %rax**

# Data Dependencies: 1 Nop

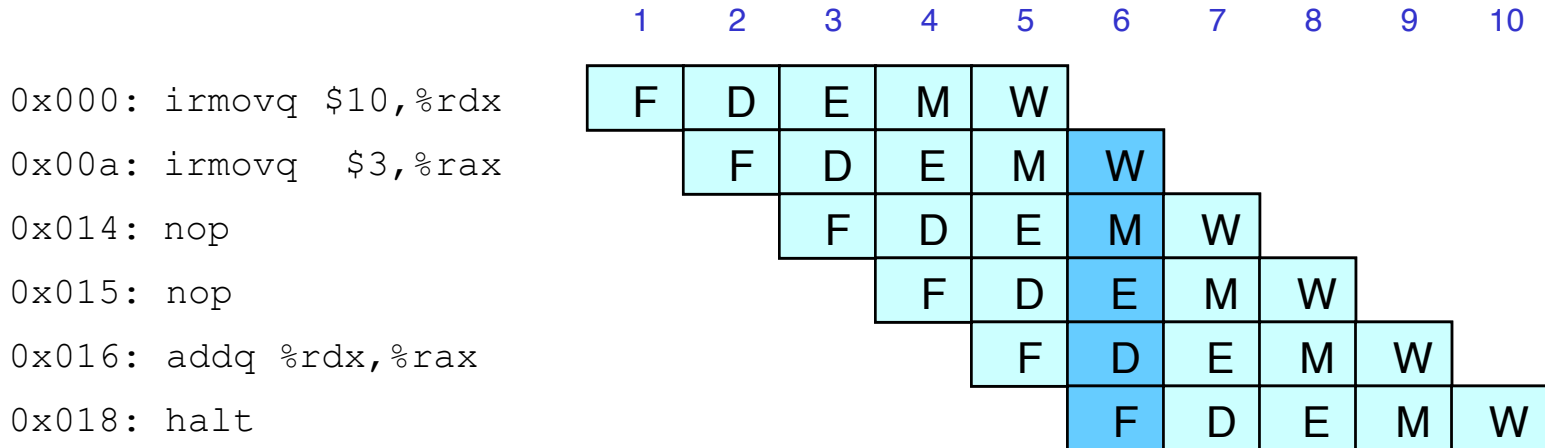
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**addq still reads wrong %rdx and %rax**

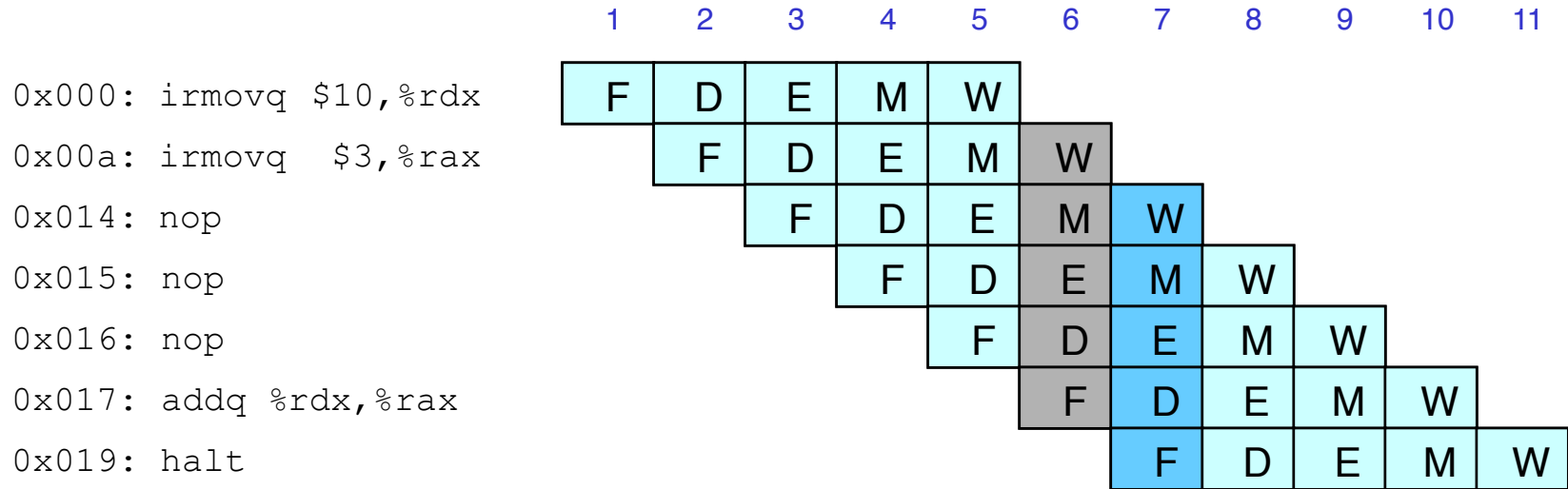


# Data Dependencies: 2 Nop's



**addq reads the correct %rdx,  
but %rax still wrong**

# Data Dependencies: 3 Nop's

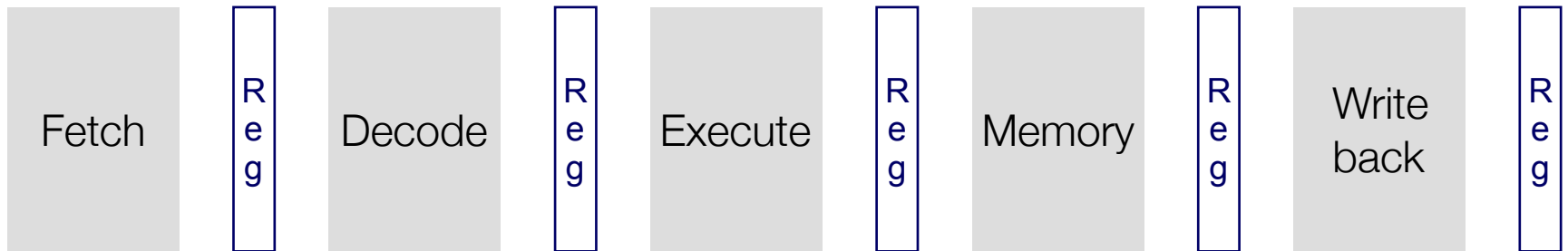


**addq reads the correct %rdx  
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# Hardware Generated Nops (Bubble and Stalling)

Can we have the hardware automatically generates a nop?

- Why is it good for the hardware to do so anyways?

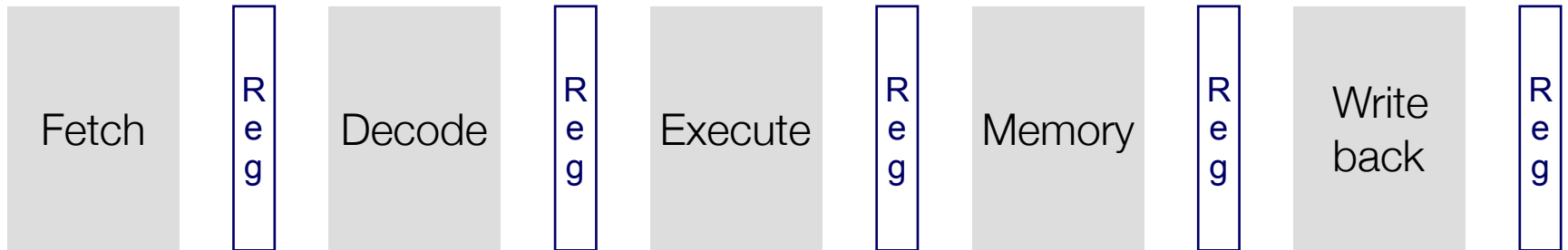


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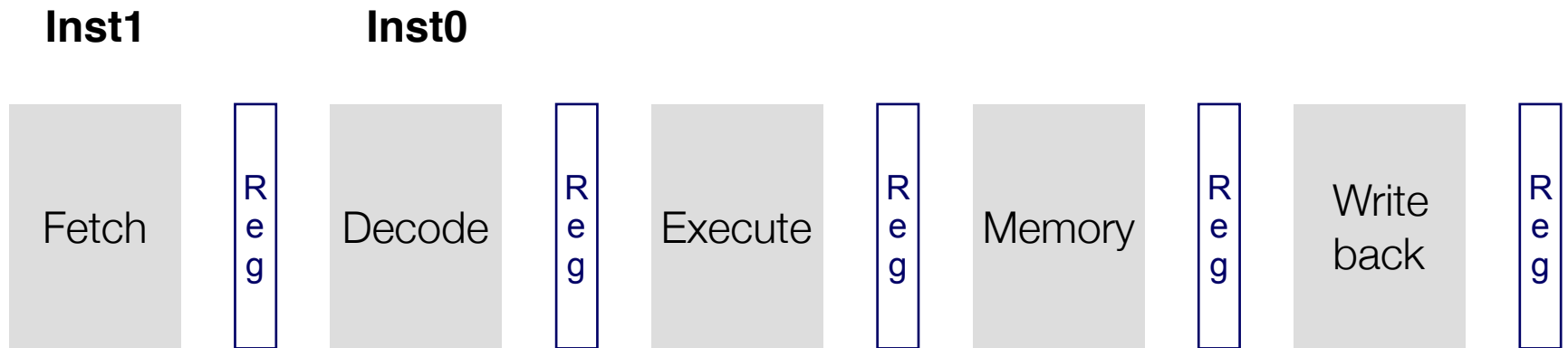
**Inst0**



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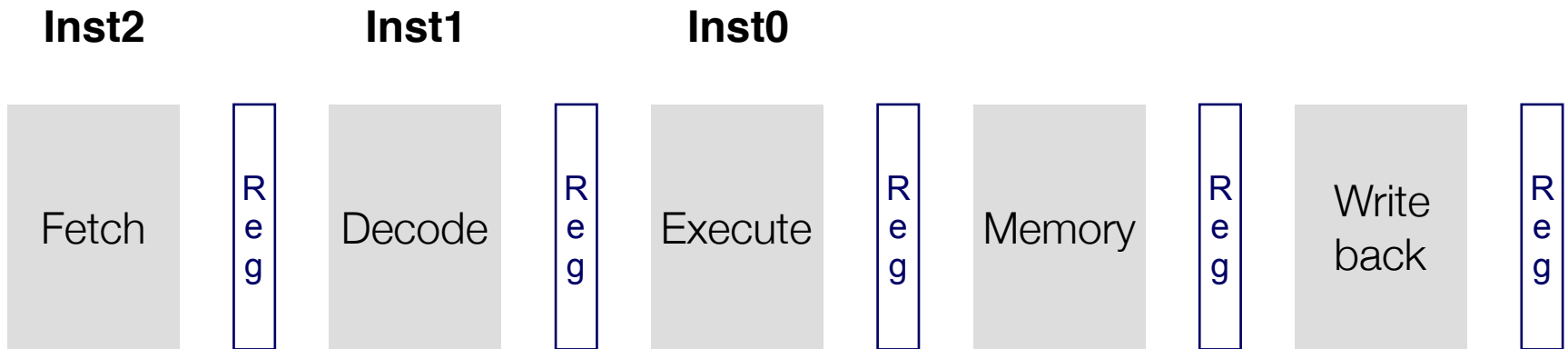
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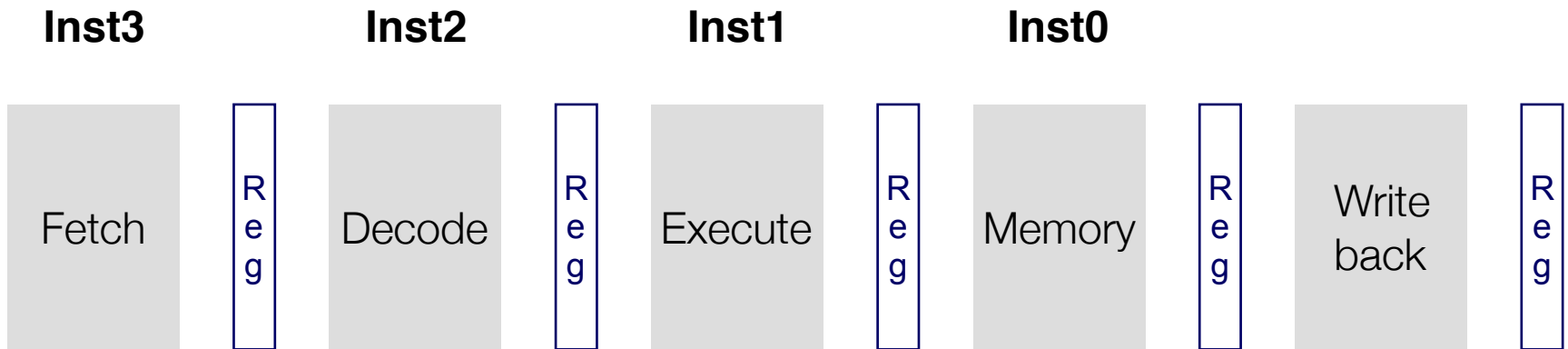
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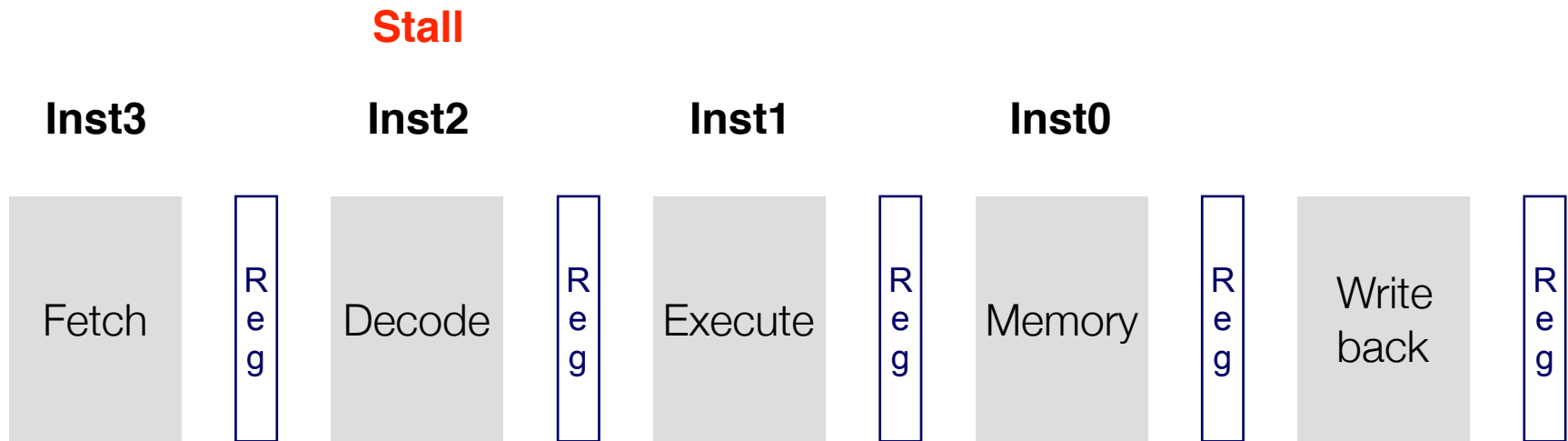
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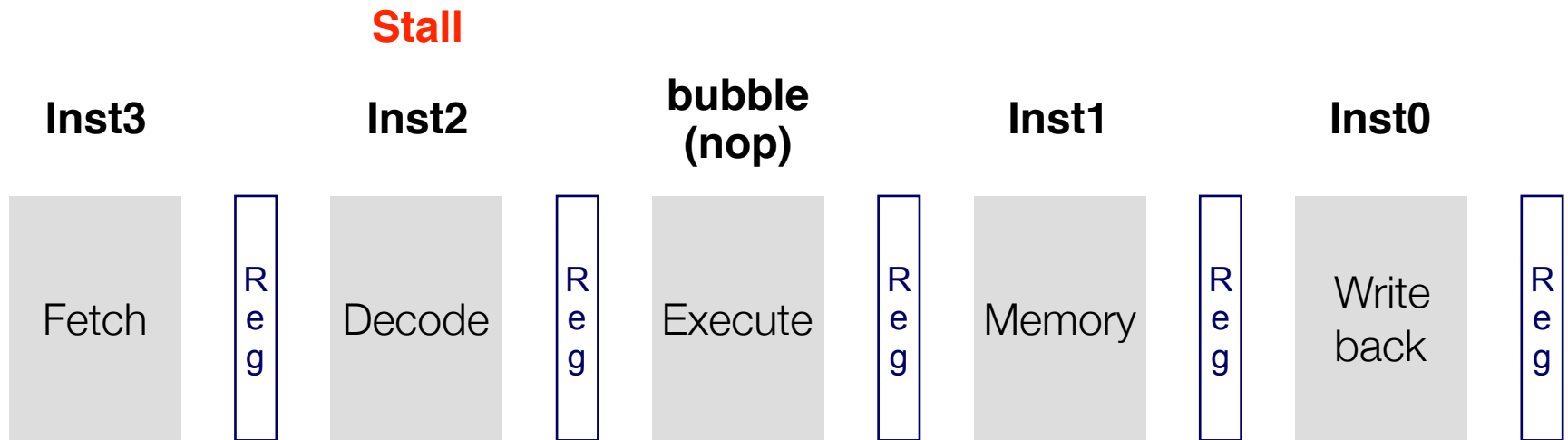




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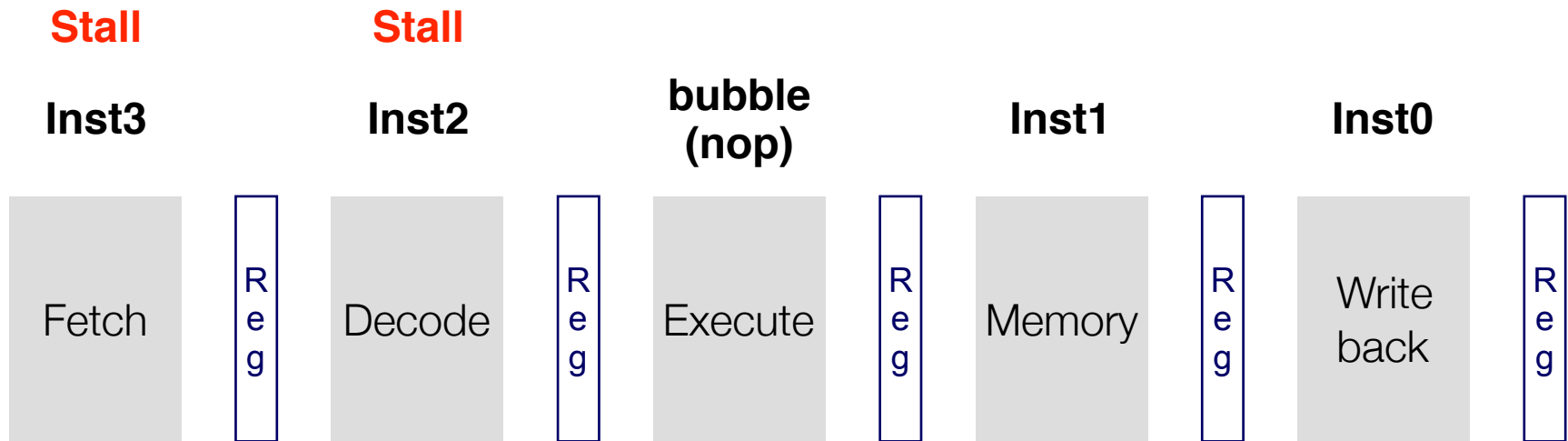
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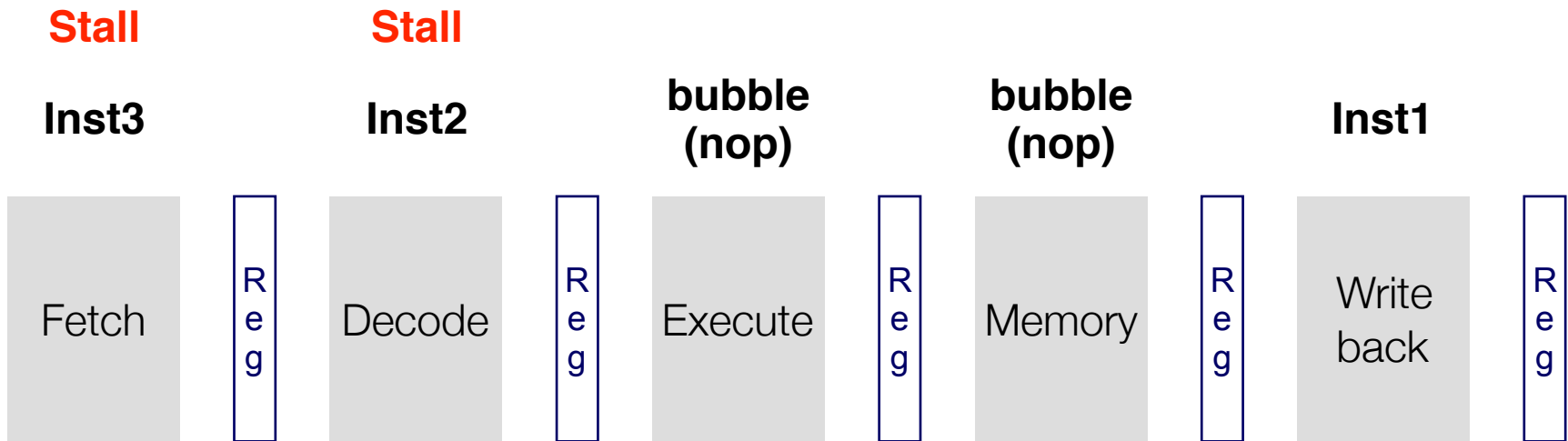
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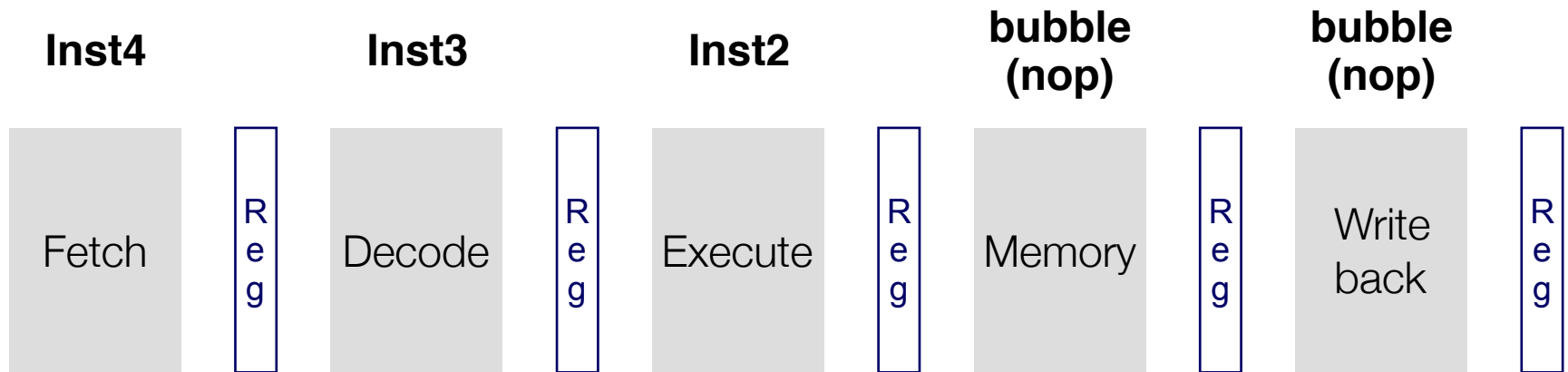
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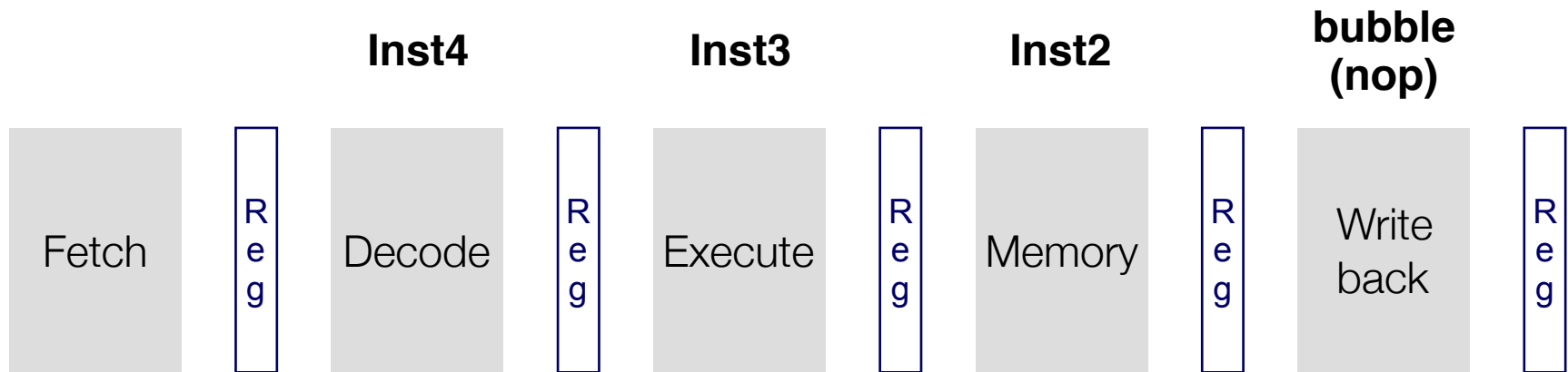
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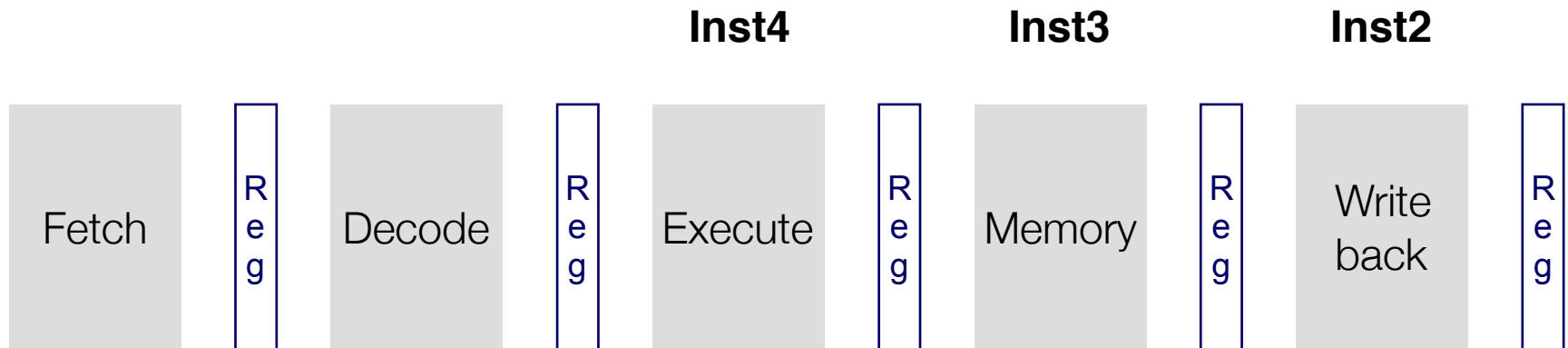
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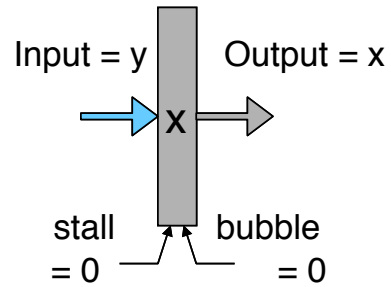
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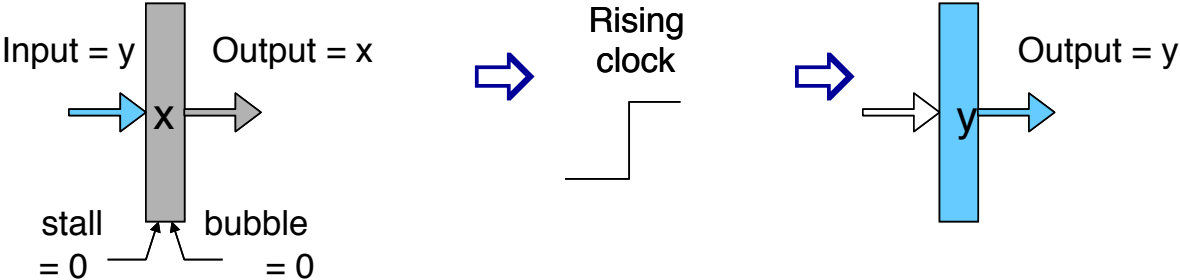
**Normal**





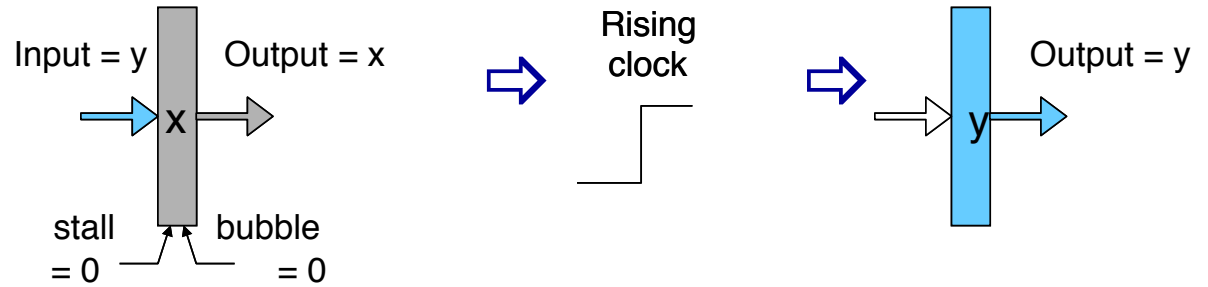
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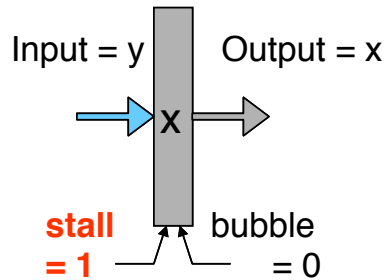


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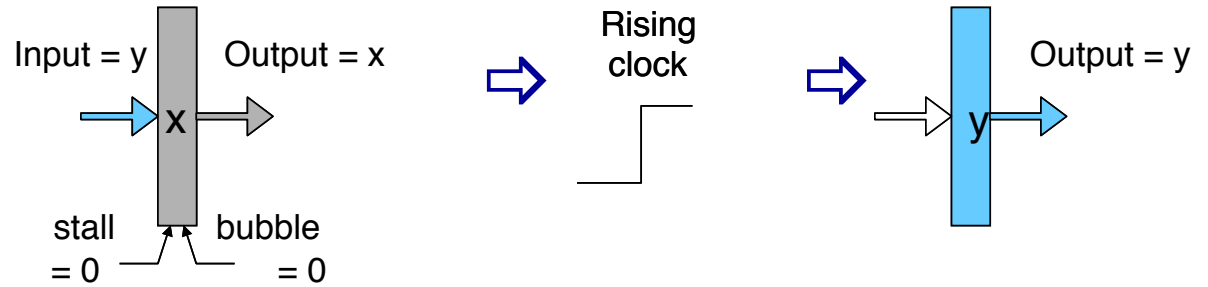


**Stall**

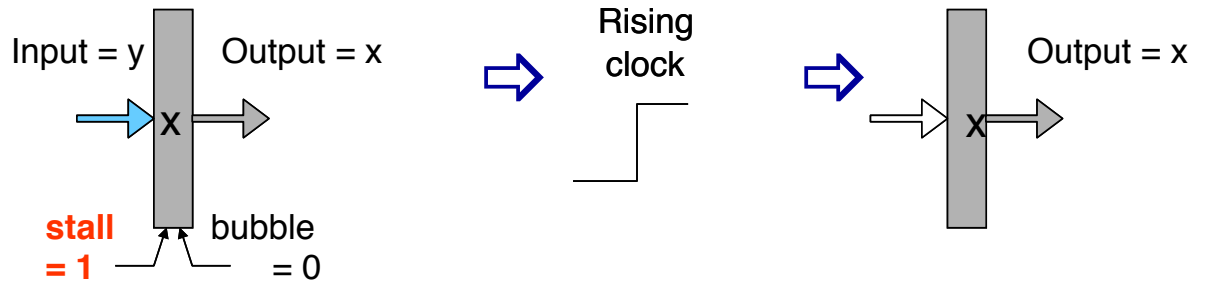


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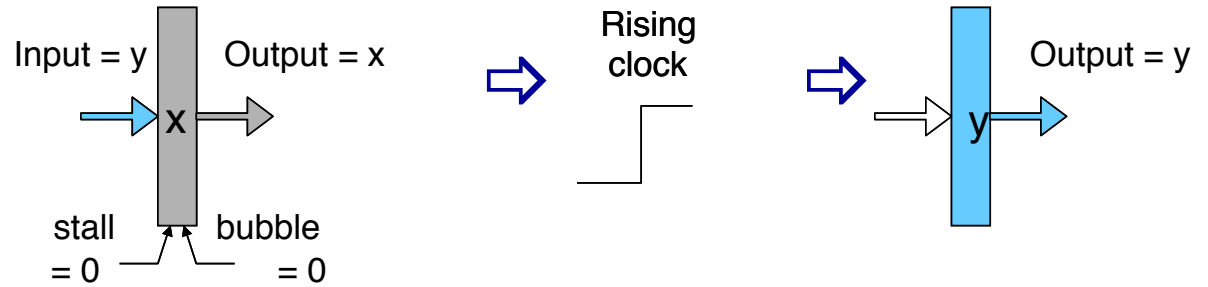


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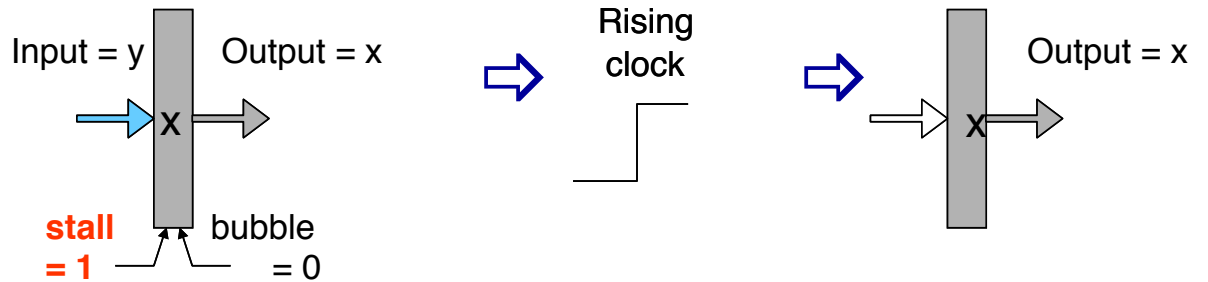


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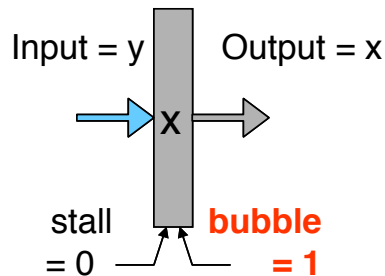
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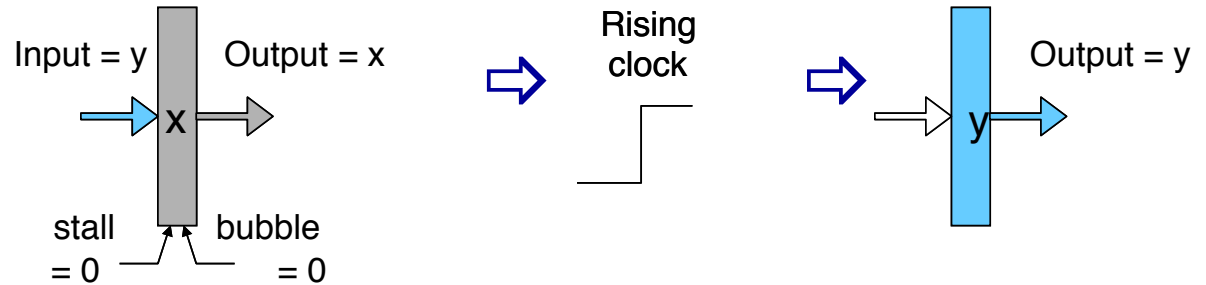


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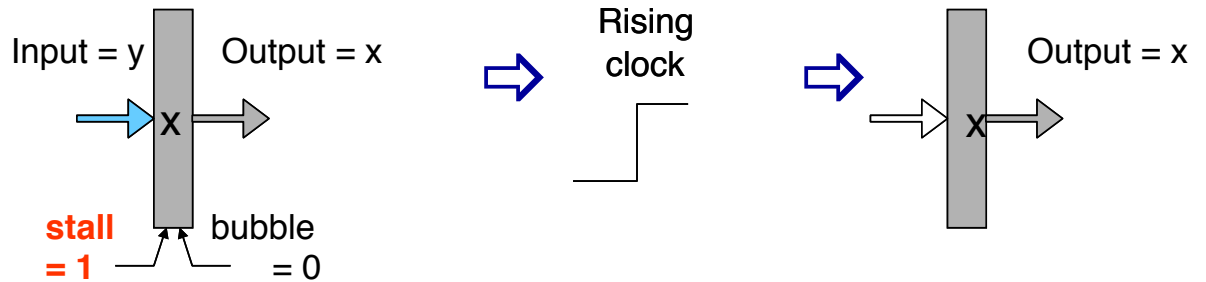


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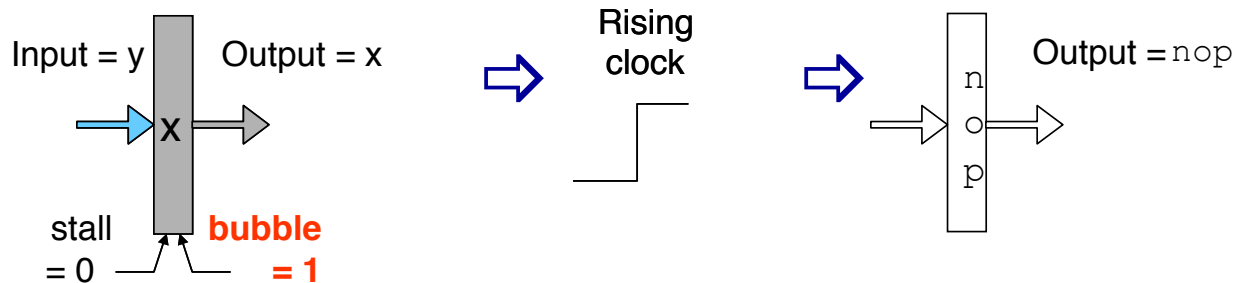
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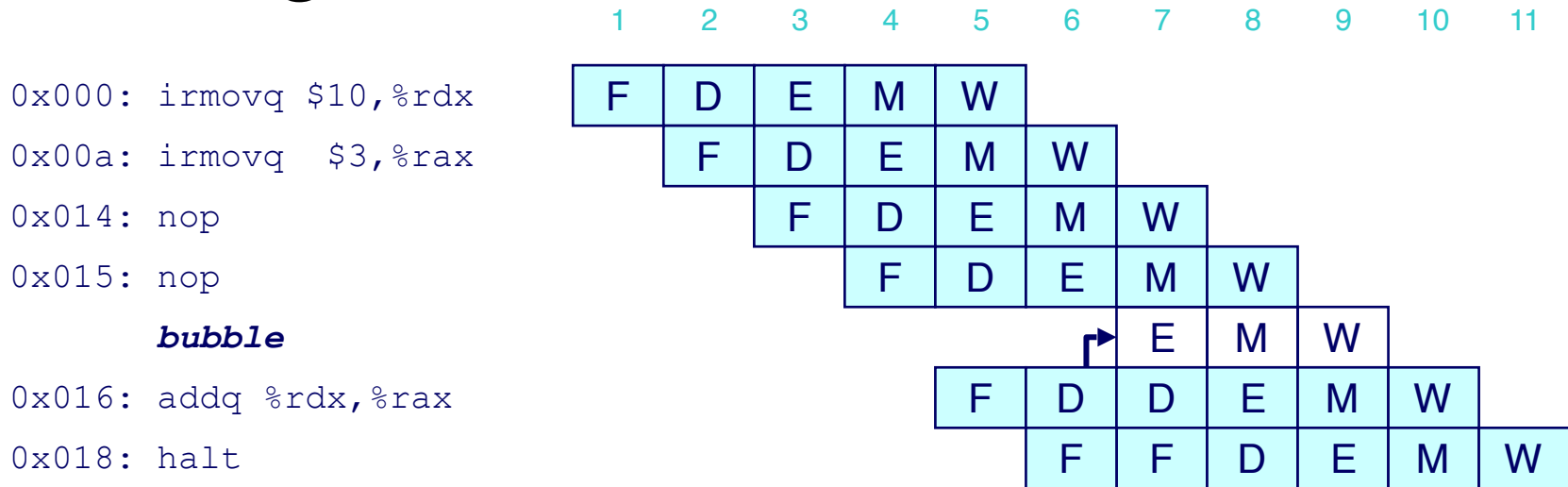
**Stall**



**Bubble**



# Detecting Stall Condition



- Using a “**scoreboard**”. Each register has a bit.
- Every instruction that writes to a register sets the bit.
- Every instruction that reads a register would have to check the bit first.
  - If the bit is set, then generate a bubble
  - Otherwise, free to go!!

# Data Forwarding

## Naïve Pipeline

- Register isn't written until completion of write-back stage
- Source operands read from register file in decode stage
- The decode stage can't start until the write-back stage finishes

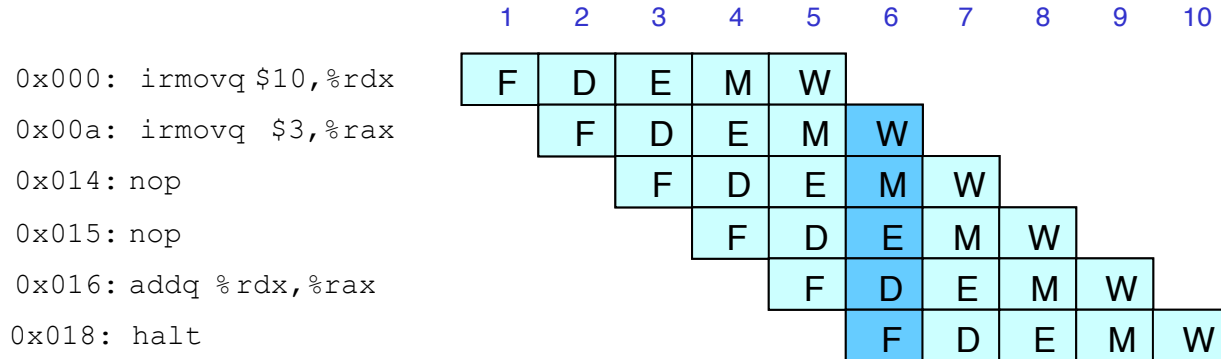
## Observation

- Value generated in execute or memory stage

## Trick

- Pass value directly from generating instruction to decode stage
- Needs to be available at end of decode stage

# Data Forwarding Example

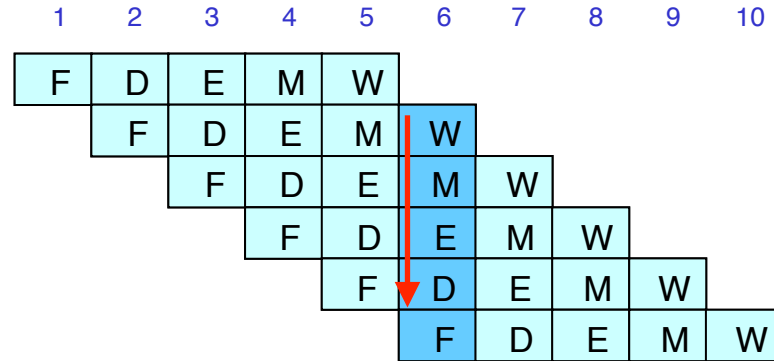


- `irmovq` writes `%rax` to the register file at the end of the write-back stage
- But the value of `%rax` is already available at the beginning of the write-back stage
- Forward `%rax` to the decode stage of `addq`.



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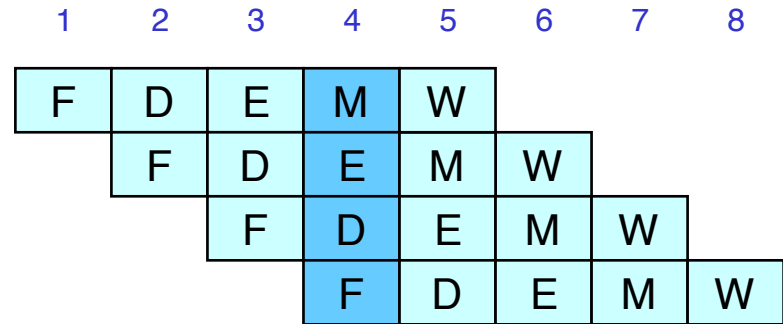
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# Data Forwarding Example #2

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Register `%rdx`

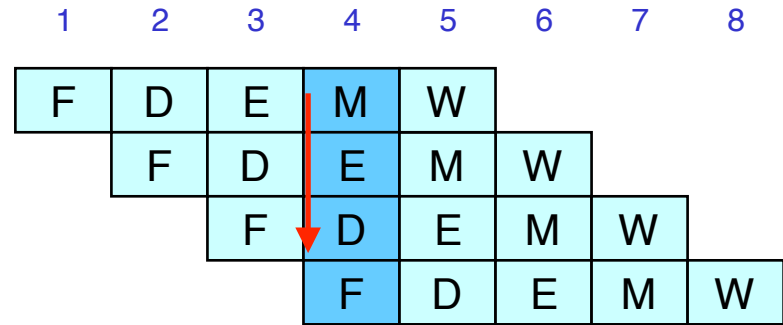
- Forward from the memory stage

Register `%rax`

- Forward from the execute stage

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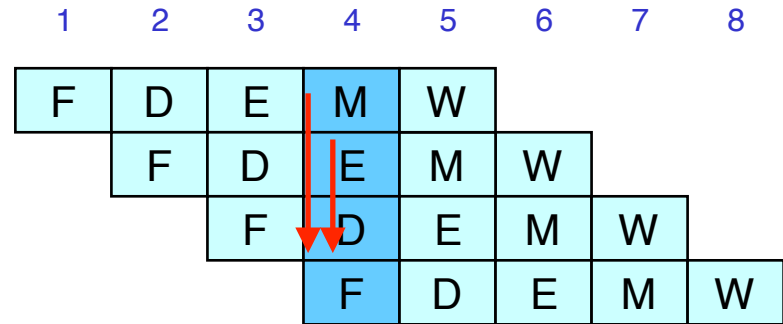
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# Out-of-order Execution

- Compiler could do this, but has limitations
- Generally done in hardware

Long-latency instruction.  
Forces the pipeline to stall.

**r0** = r1 + r2  
**r3** = MEM[**r0**]  
r4 = **r3** + r6  
r7 = r5 + r1  
...



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Is this correct?



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“**Tomasolu Algorithm**” is the algorithm that is most widely implemented in modern hardware to get out-of-order execution right.