

Restricting Control Flow During Speculative Execution with Venkman

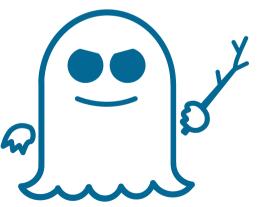
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Picture from the Internet

Speculative Execution

- Feature to improve processor performance
 - Equipped in x86, ARM, POWER, etc
- Execute instructions prior to knowing if they are needed
 - Restore and re-execute on mis-speculation
 - Leave observable side effects
- Vulnerable to sophisticated attacks!



Spectre Attacks

Variant 1: exploit conditional branches

- Direction prediction using PHT
- Mitigations: fence, data dependence

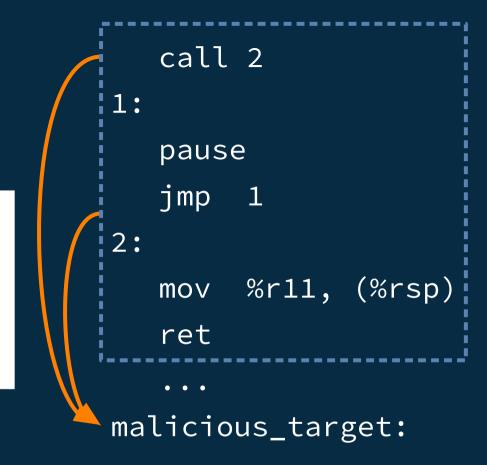
Variant 2: exploit indirect branches

- Target prediction using BTB and RSB
- Mitigations: microcode, Retpoline

```
if (x < arr1_size) {
    y = arr1[x];
}</pre>
```

```
(*func_ptr)(); // return;
if (x < arr1_size) {
    load_fence();
    y = arr1[x];
}</pre>
```

What if **direct branch targets** can also be poisoned?



Retpoline becomes vulnerable too!

Venkman: Our Solution!

• Defense against BTB & RSB poisoning

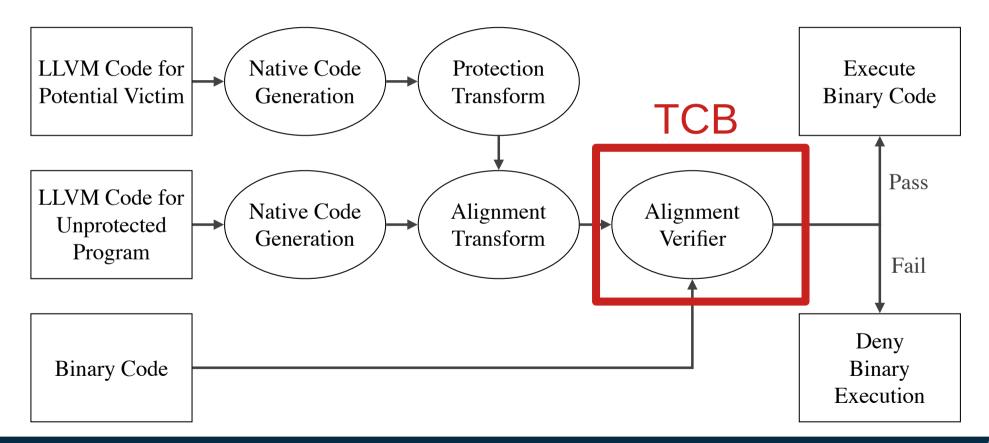
- Aligned control-flow transfer targets
- Protective instructions not bypassed
- Broad threat model
 - Any program can be a potential attacker!
 - Require whole-system instrumentation



Outline

- Design
- Implementation
- Security Evaluation
- Space & Performance Evaluation
- Conclusions & Future Work

Venkman System Architecture



Venkman Transformations

Alignment transformations

Code padding & alignment

Core of Venkman

- Bit-masking control data

Protection transformations

- Spectre protection

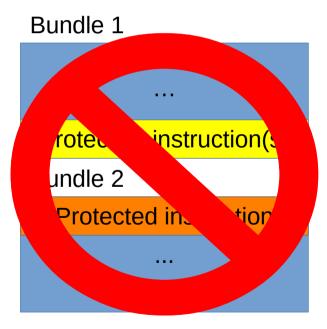
Code Padding & Alignment

- Transform basic blocks
 into bundles
 - Groups of Instructions sized and aligned at 2^s bytes
 - Split large BBs
 - Pad NOPs to small BBs
- Function calls at the end of bundle

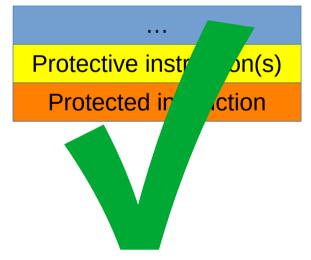
BB1	Bundle1
0x00: add %r3, %r3, -1 0x00: cmp %r3, 1 0x04: jgt BB1	S = 4 0x00: nop 0x04: add %r3, %r3, -1 0x08: cmp %r3, 1 0x0c: jgt Bundle1
BB2	Bundle2
0x08: mul %r3, %r3, 10 0x0c: add %r4, %r2, -2 0x10: add %r3, %r3, 36 0x14: call printf	0x10: mul %r3, %r3, 10 0x14: add %r3, %r2, -2 0x18: add %r3, %r3, 36 0x1c: call printf
0x18: add %r3, %r4, 8 0x1c: ret	Bundle3
	0x20: nop 0x24: nop 0x28: add %r3, %r4, 8 0x2c: ret

Code Padding & Alignment

Honor co-location requirements

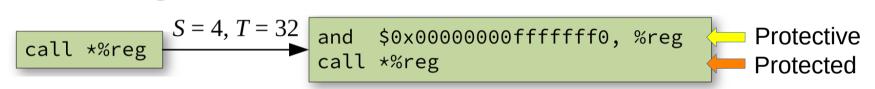


Bundle 1

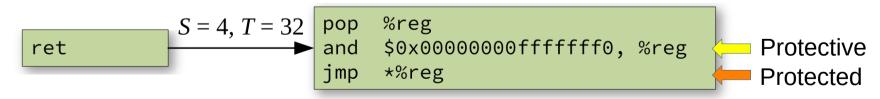


Bit-Masking Control Data

- Clear lower *S* bits
- Clear higher (64 T) bits

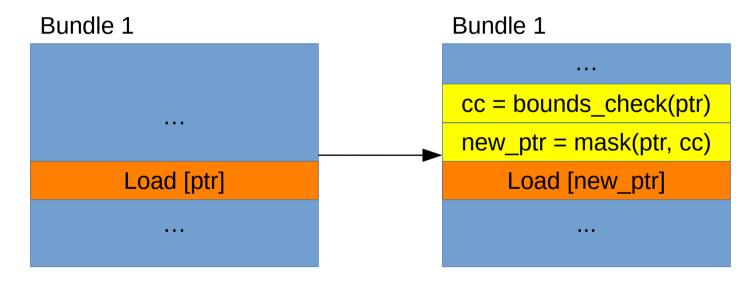


Transform branches w/ in-memory target



Spectre Protection

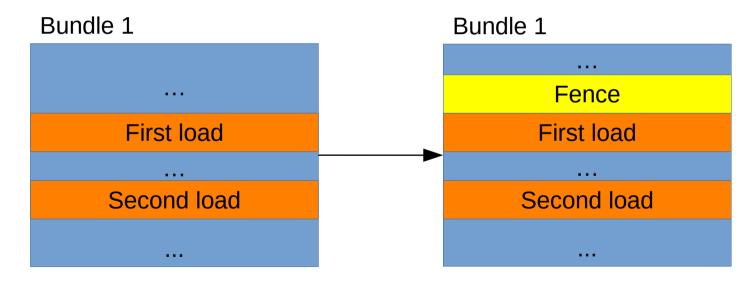
• Insert Spectre-resistant SFI [1]



[1] X. Dong et al. Spectres, Virtual Ghosts, and Hardware Support. In HASP'18.

Spectre Protection

Insert fences



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Implementation

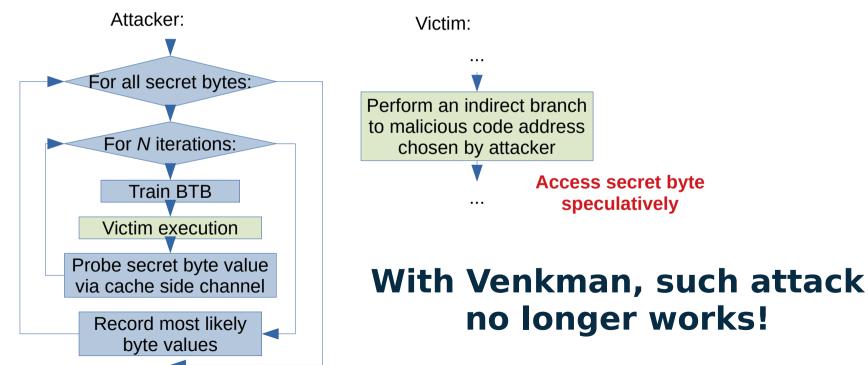
- Implemented on POWER architecture
- Extended LLVM with MachineFunctionPasses
- **32-byte bundles (***S* = 5**)**
- Code segment at first 32 TB (T = 45)
- Use EIEIO as fence Enforce In-order Execution of I/O
- Use dummy SFI

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Security Evaluation

Proof-of-concept Spectre V2 attack on POWER



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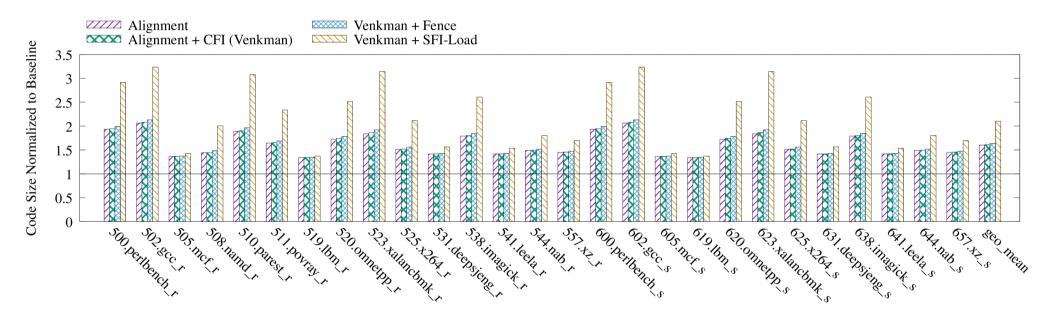
Experimental Setup

- Hardware specifications
 - 64-bit IBM POWER8
 - 20 cores, 8 threads/core
 - 4.1 GHz
 - 64 GB RAM
- Configurations
 - Baseline
 - Alignment only
 - Alignment + CFI (Venkman)
 - Venkman + Fence
 - Venkman + SFI-Load

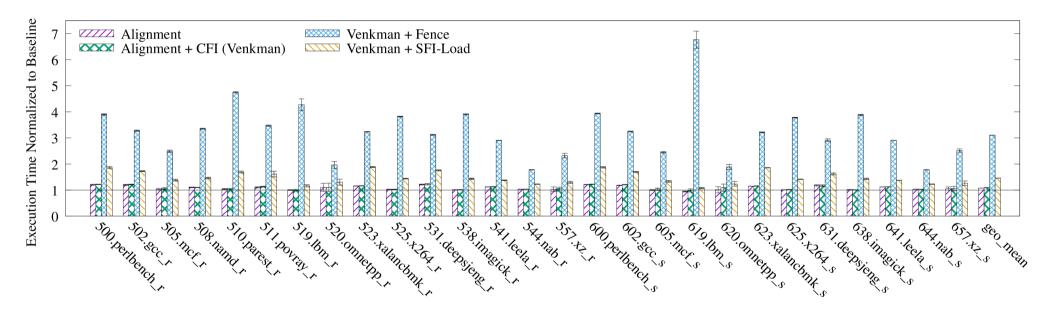
- Software specifications
 - CentOS 7 w/ Linux 3.10.0
 - LLVM/Clang 4.0.1

- Benchmarks & applications
 - SPEC CPU 2017
 - Nginx 1.15.8
 - GnuPG 1.4.23
 - ClamAV 0.92

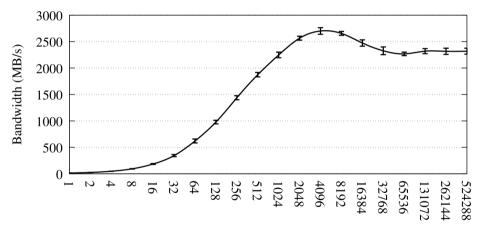
Code Size Overhead on SPEC CPU 2017



Performance Overhead on SPEC CPU 2017

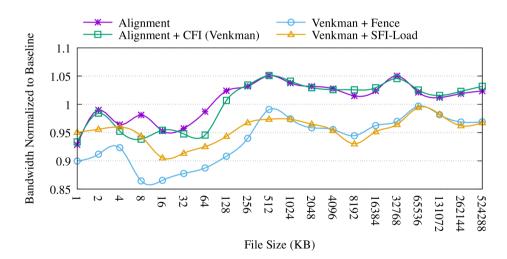


Nginx File Transfer Rate



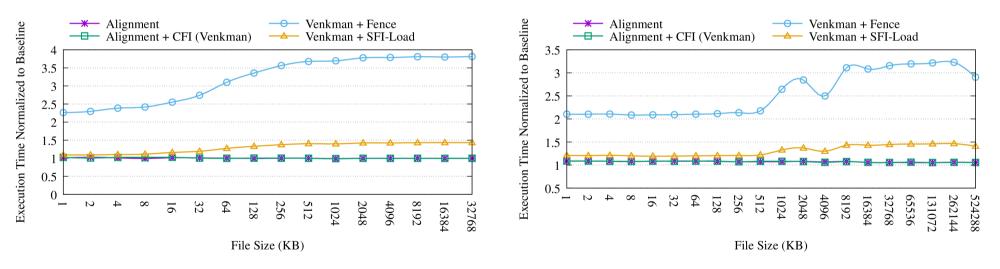
File Size (KB)

Baseline



Venkman Normalized to Baseline

GnuPG & ClamAV Overhead



GnuPG Encryption

ClamAV

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Conclusions

- Venkman mitigates BTB & RSB poisoning
- When protecting fences, Venkman exhibits
 - 1.64x average space overhead
 - 2.97x average performance overhead
- When protecting SFI, Venkman exhibits
 - 2.13x average space overhead
 - 1.43x average performance overhead
- 61.3% space and 8.6% performance overhead for non-victim programs

Future Work

- Reduce overhead
- Port to x86 & ARM

Thank you!