

Infrastructure and Methodology for Mobile SoC Modeling

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UNIVERSITY of
ROCHESTER

Mobile Systems Today

Imaging

Computer
Vision

Graphics

Video
Processing

Stereo
Acoustic

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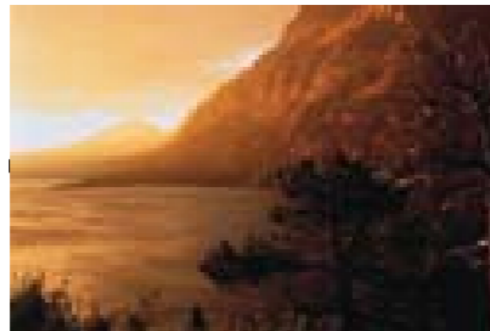
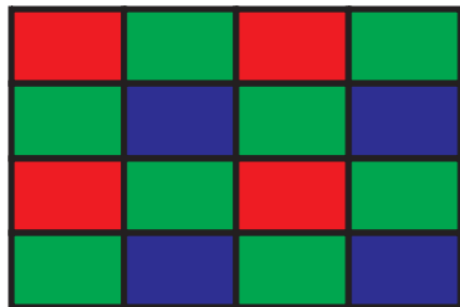
Imaging

Computer Vision

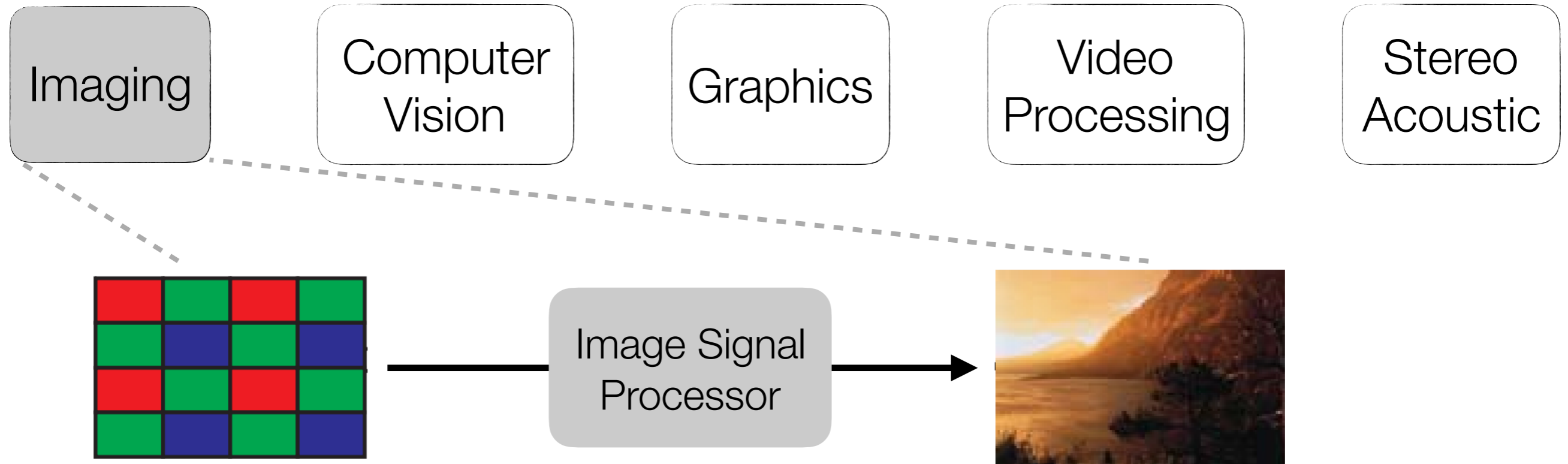
Graphics

Video Processing

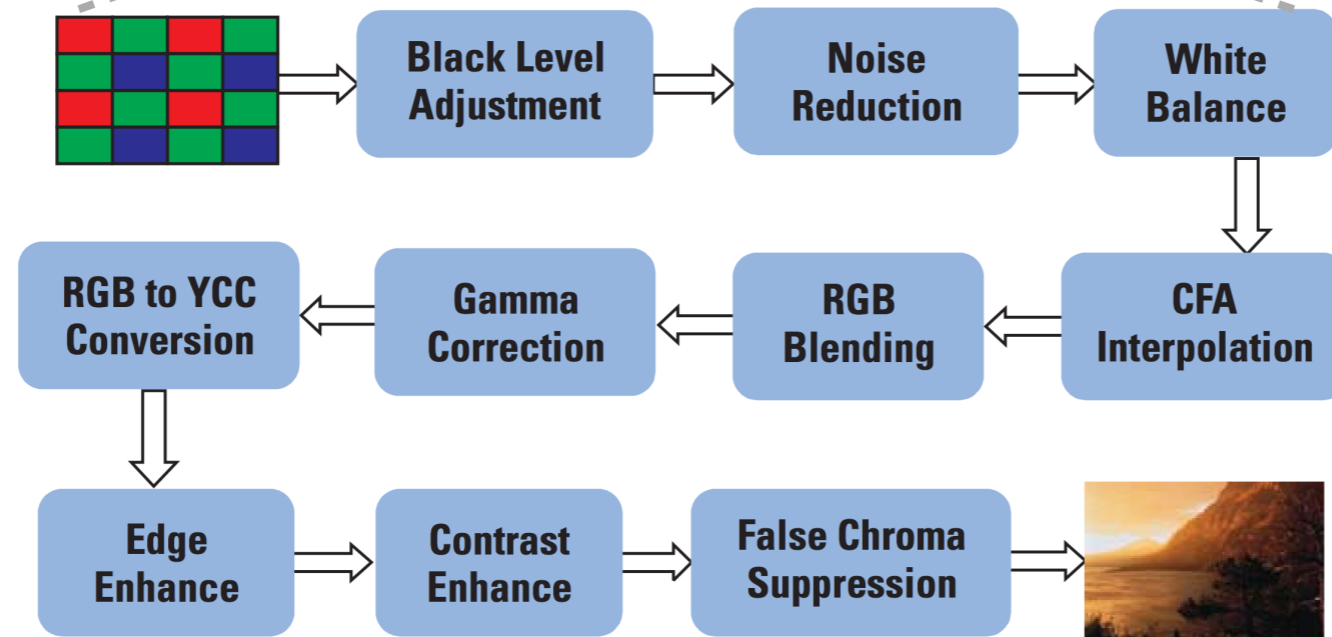
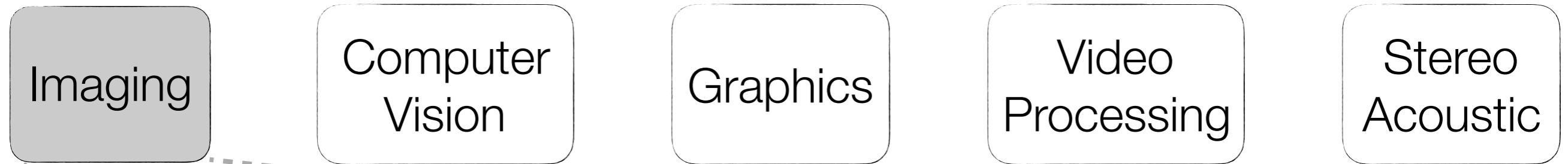
Stereo Acoustic



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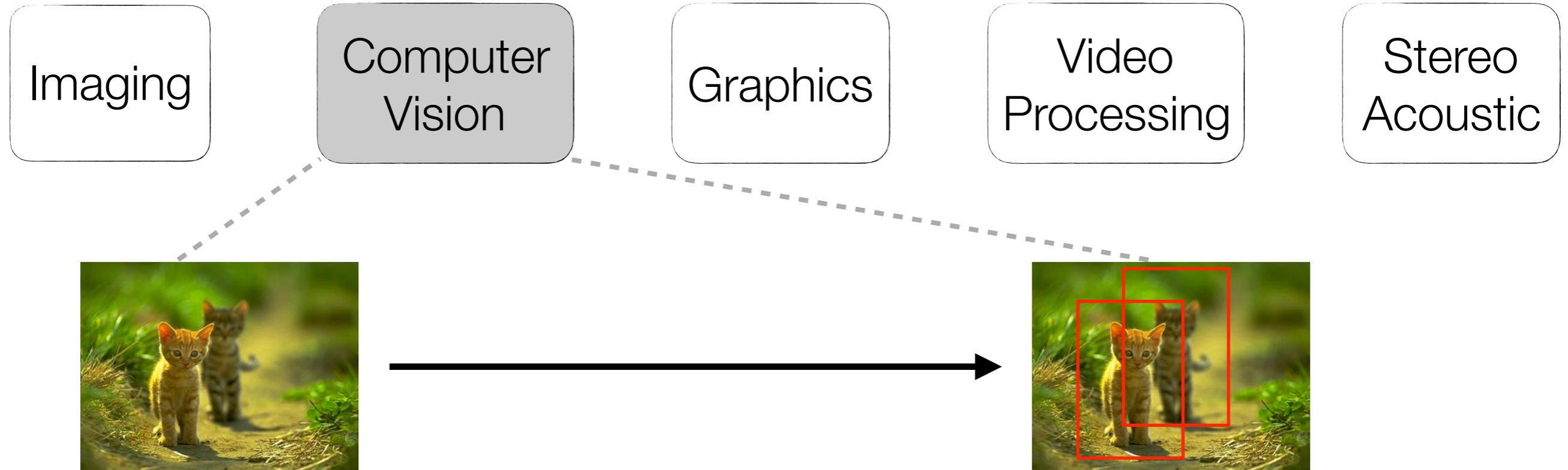
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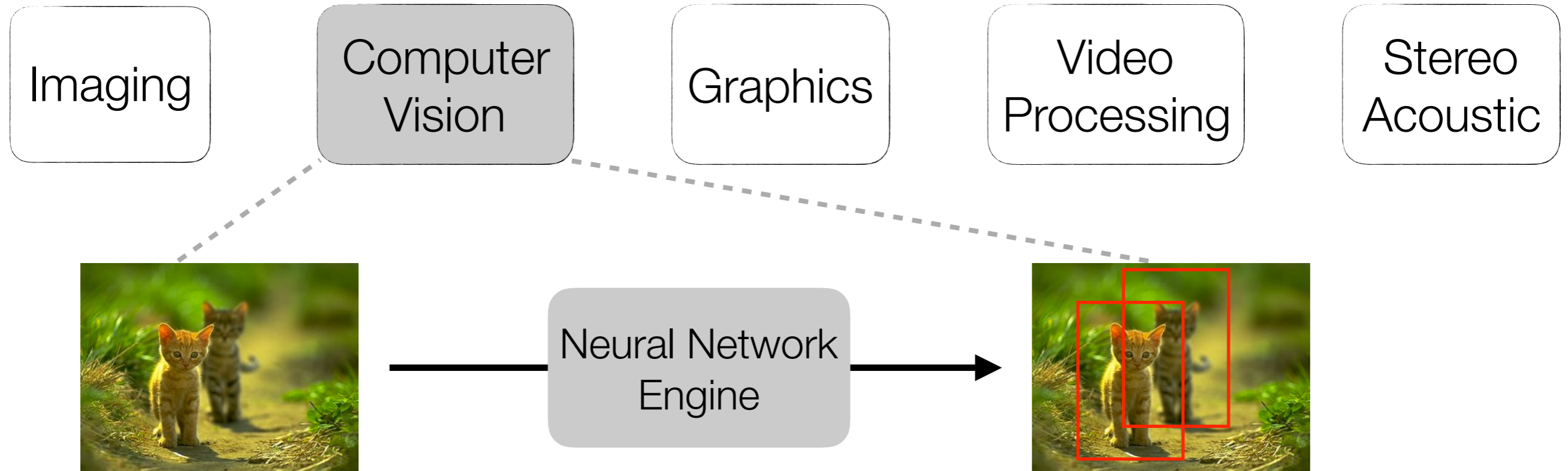
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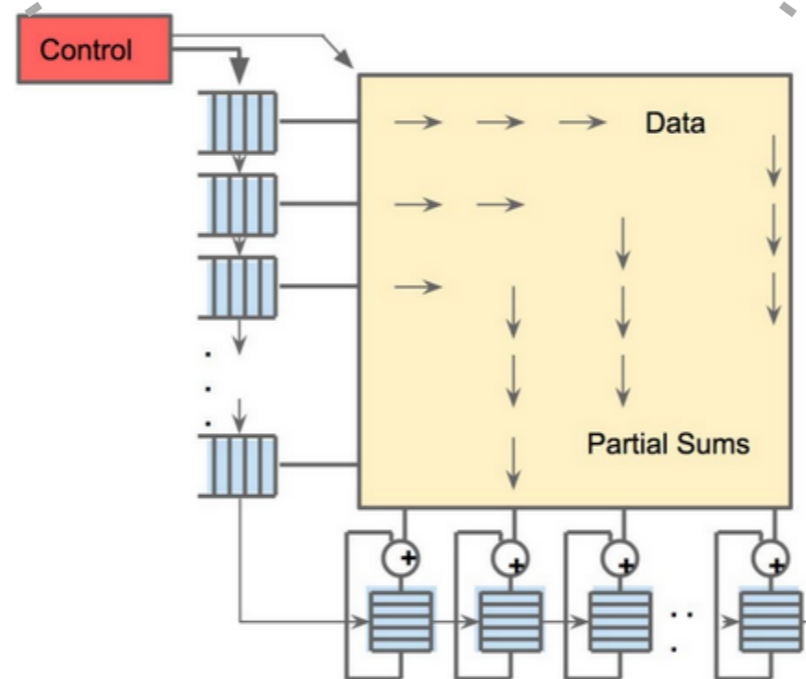
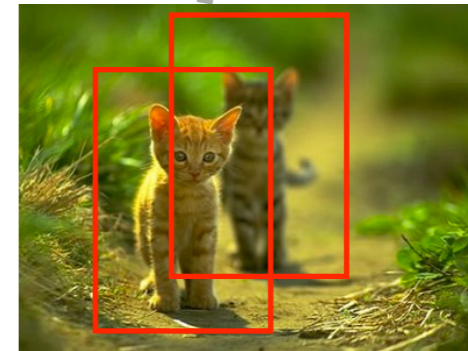
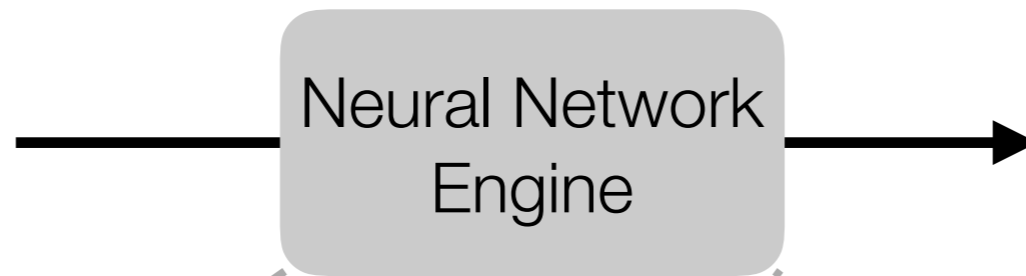
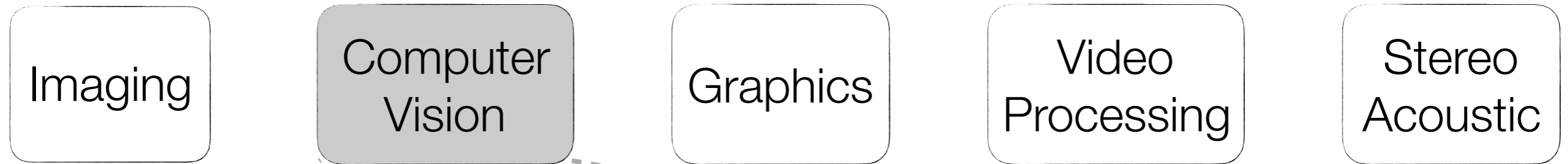
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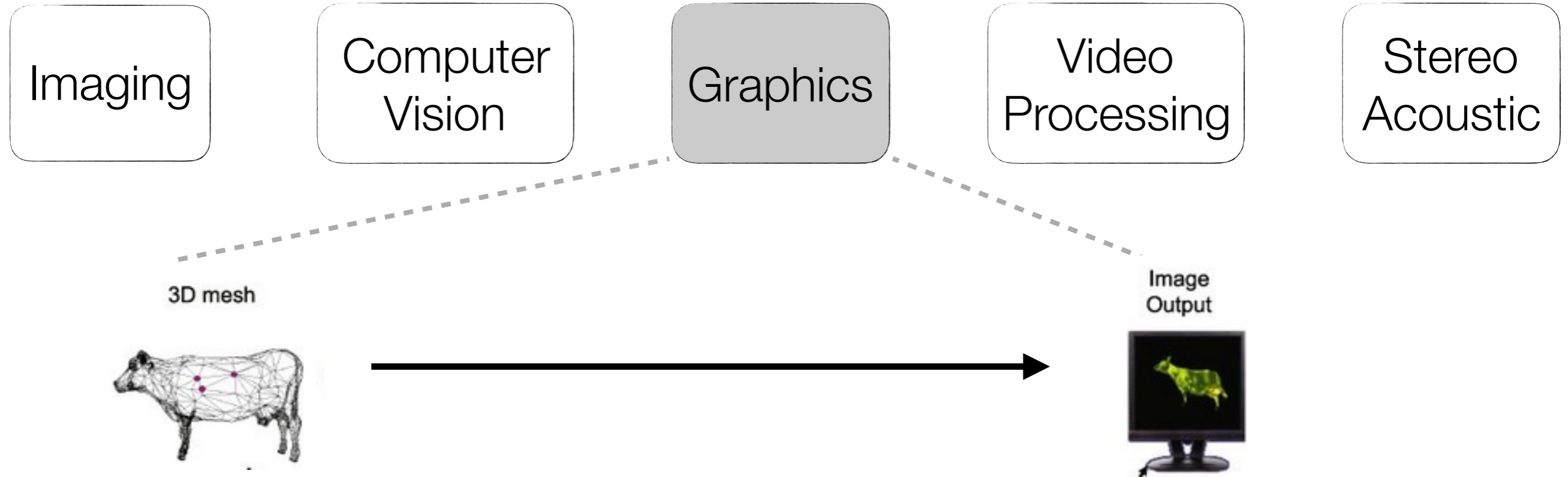
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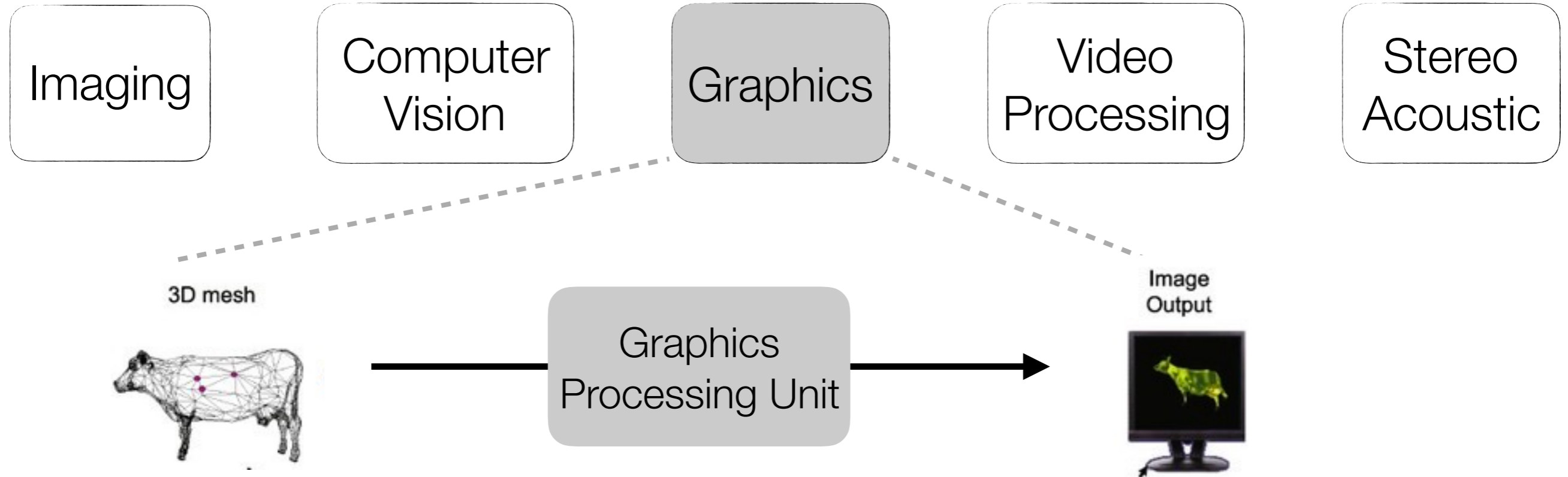
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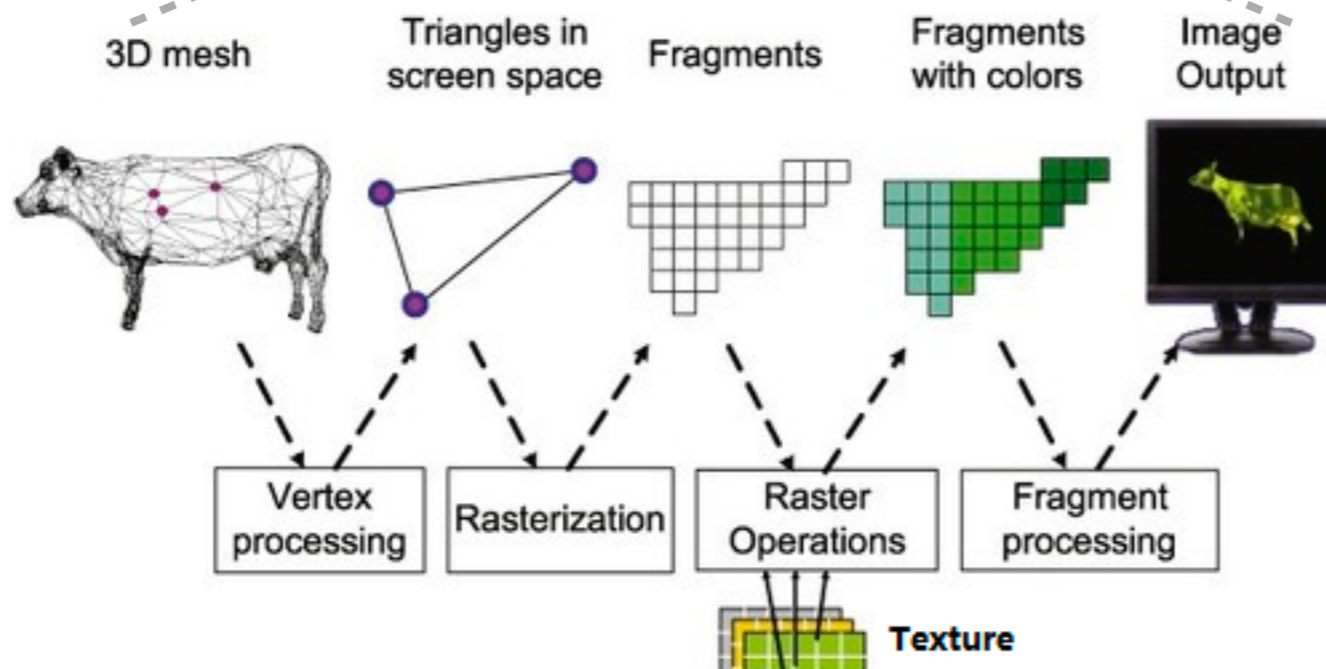
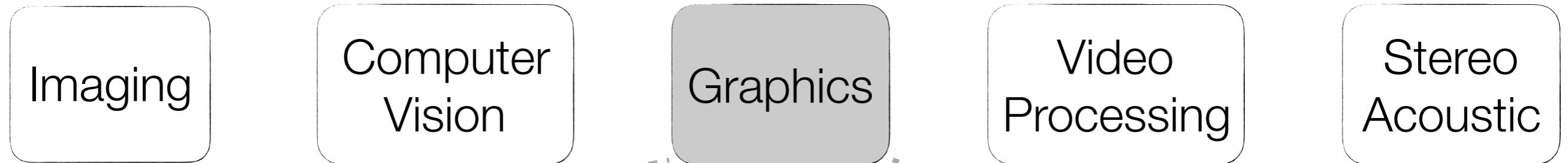
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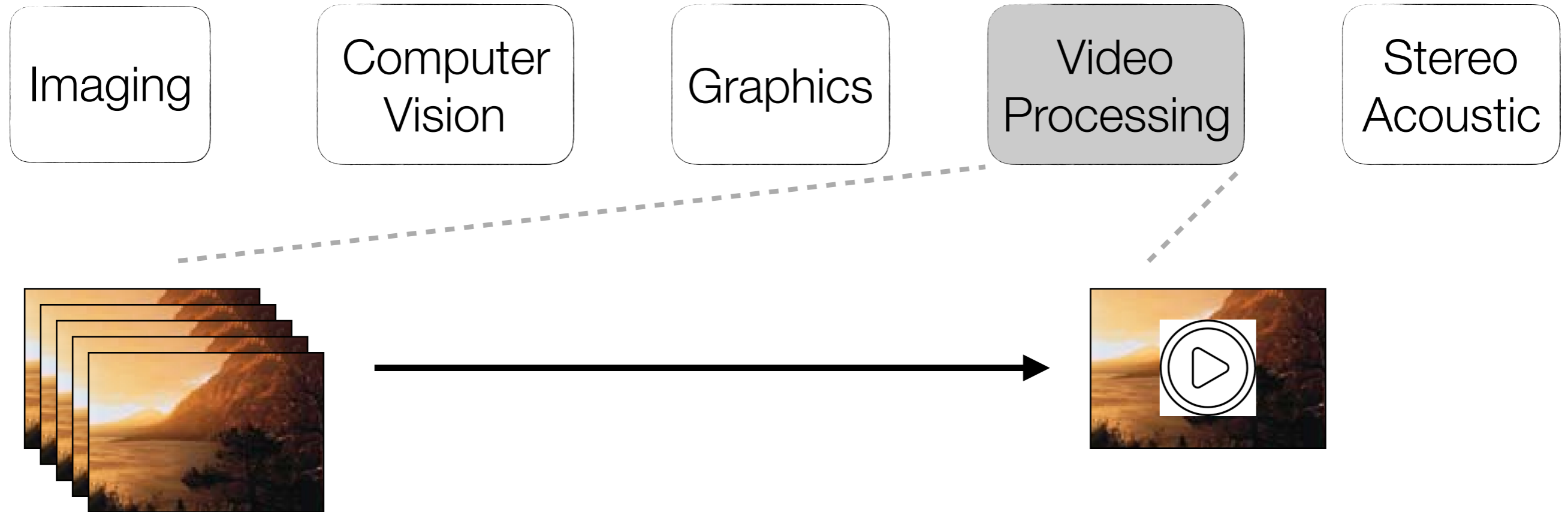
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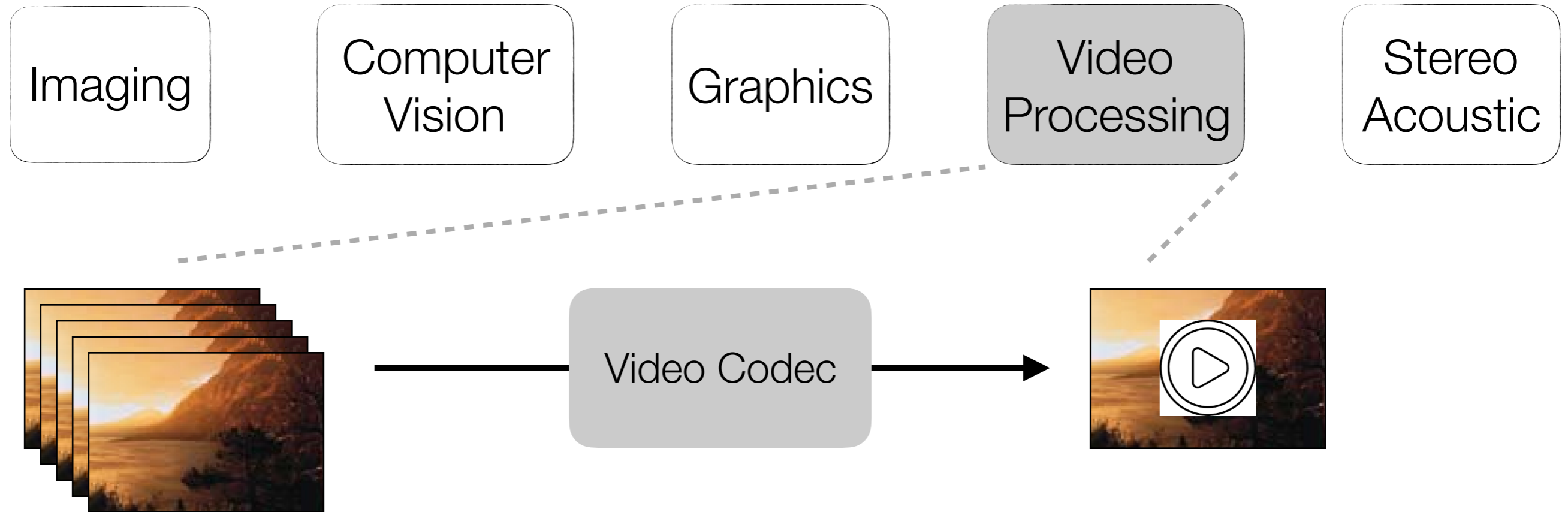
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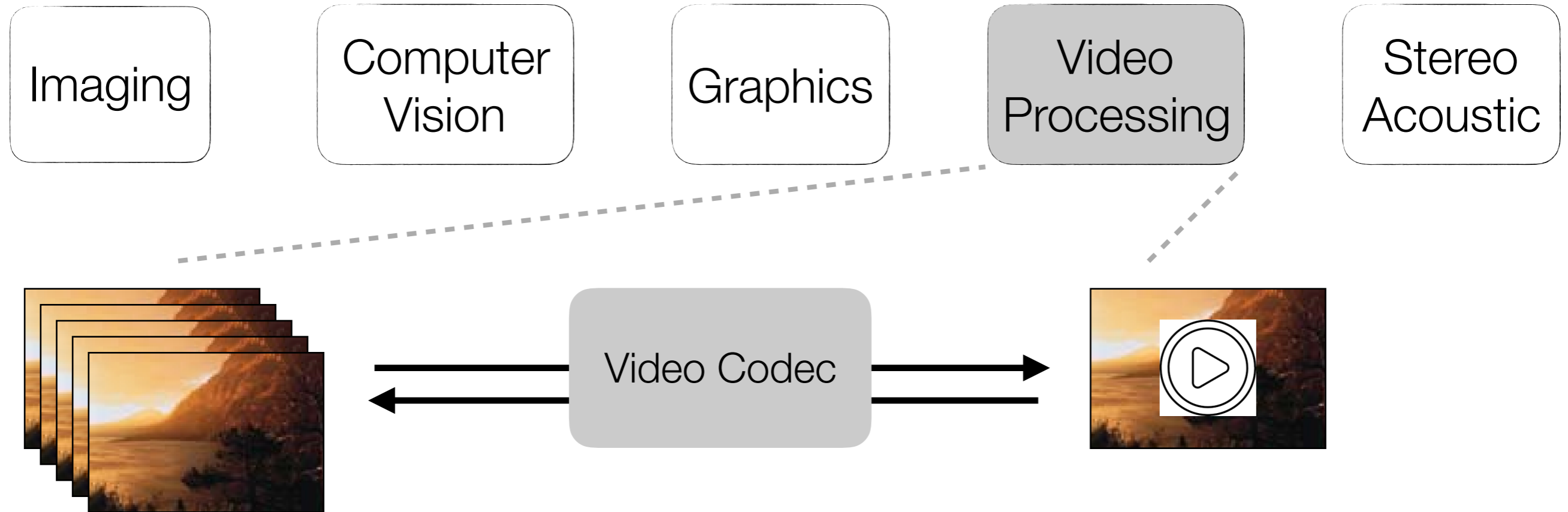
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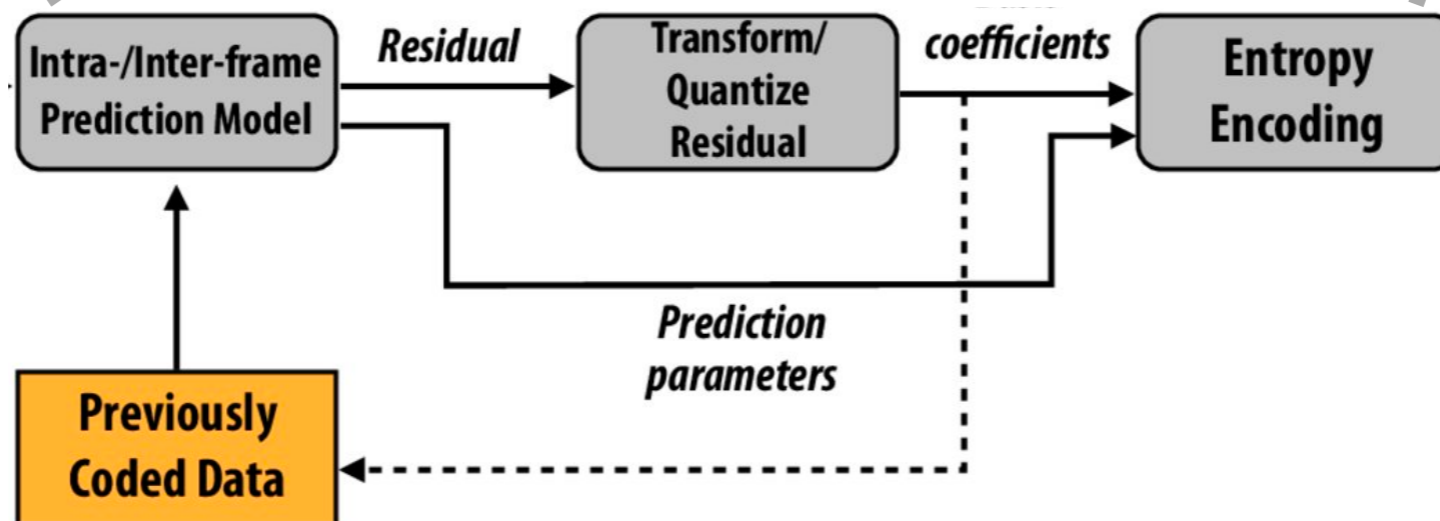
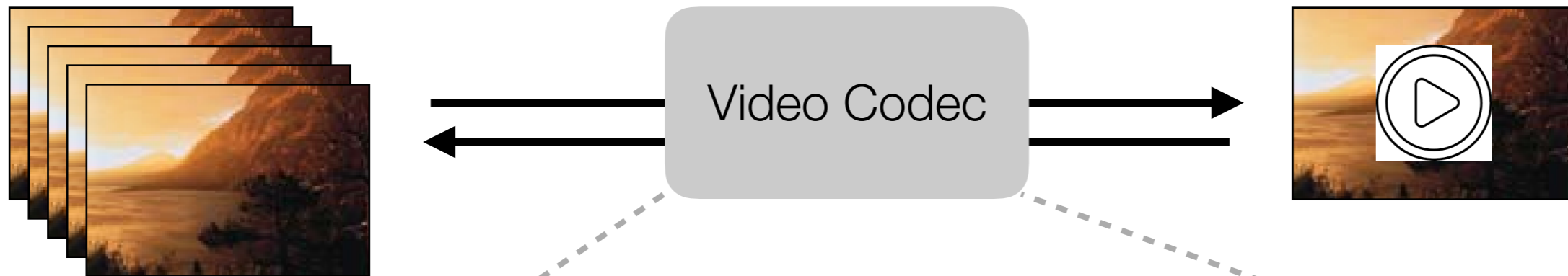
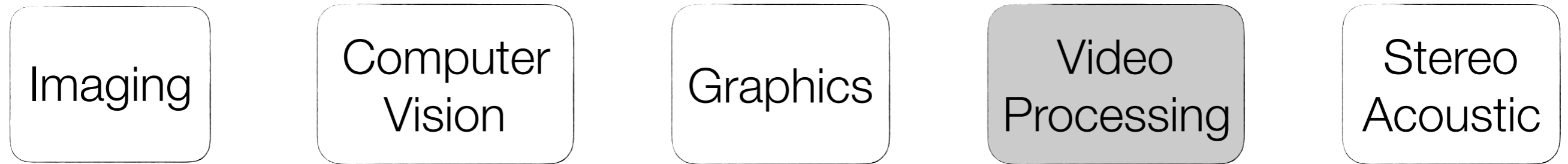
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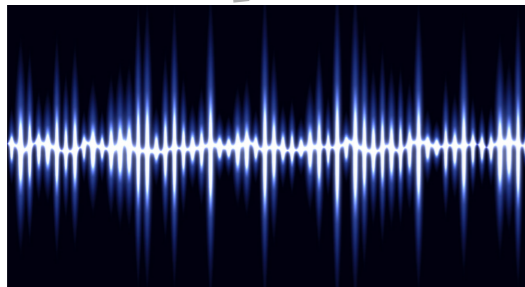
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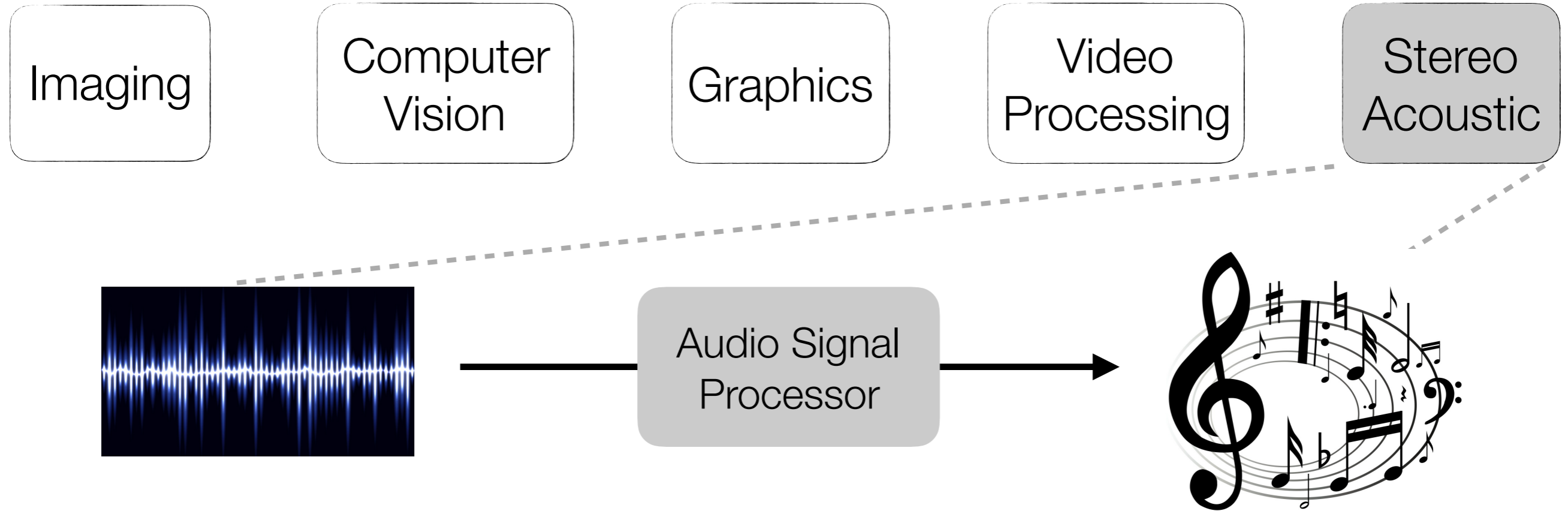
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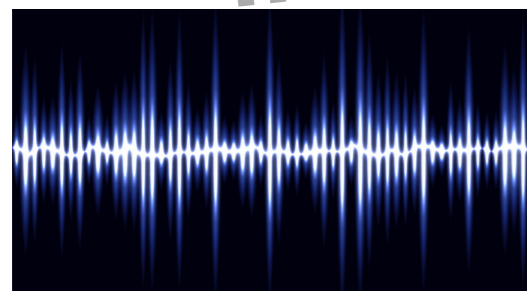
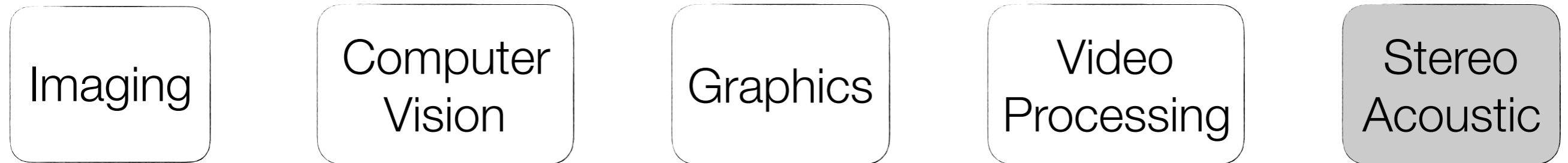
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Audio Signal Processor



Sampling Frequency must be defined

bits per sample must be defined

Analog Signal
Continuous in Time
Continuous in Amplitude

Sample & Hold

Discrete in Time
Continuous in Amplitude

Quantization

Discrete in Time
Discrete in Amplitude

Encoding

Digital Signal
Discrete in Time
Discrete in Amplitude

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Today's mobile systems are a collection of segregated sub-systems, each specialized for a domain.

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Video
Processing

Stereo
Acoustic

Image
Signal
Processor

Neural
Network
Engine

GPU

Video
Codec

Audio
Signal
Processor

Today's mobile systems are a collection of segregated sub-systems, each specialized for a domain.

Imaging

Computer
Vision

Graphics

Video
Processing

Stereo
Acoustic

Halide

OpenCV/
PyTorch

OpenGL

Fixed-
Function

Some DSP
Lang.

Image
Signal
Processor

Neural
Network
Engine

GPU

Video
Codec

Audio
Signal
Processor

Emerging Applications Integrate All Components

Camera



Headset



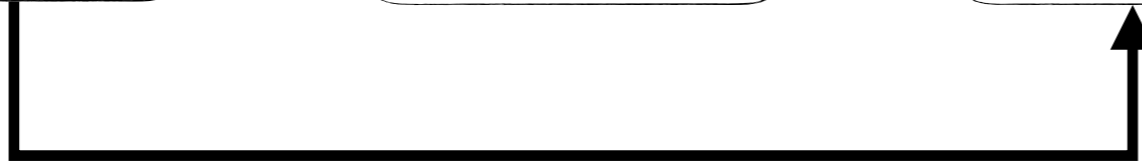
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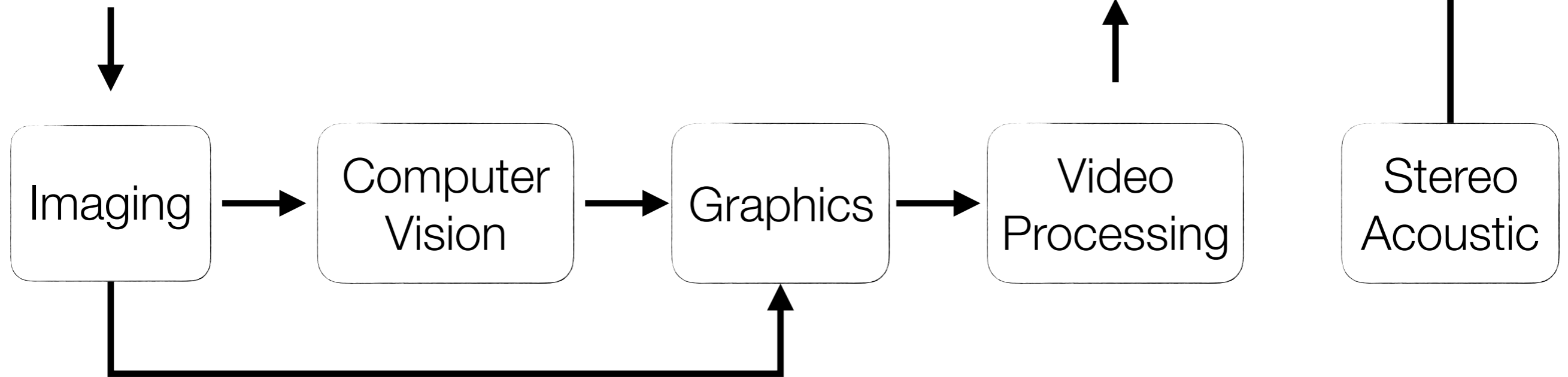


Emerging Applications Integrate All Components

Camera

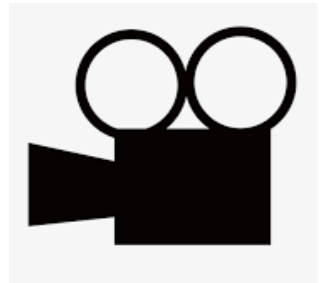


Headset

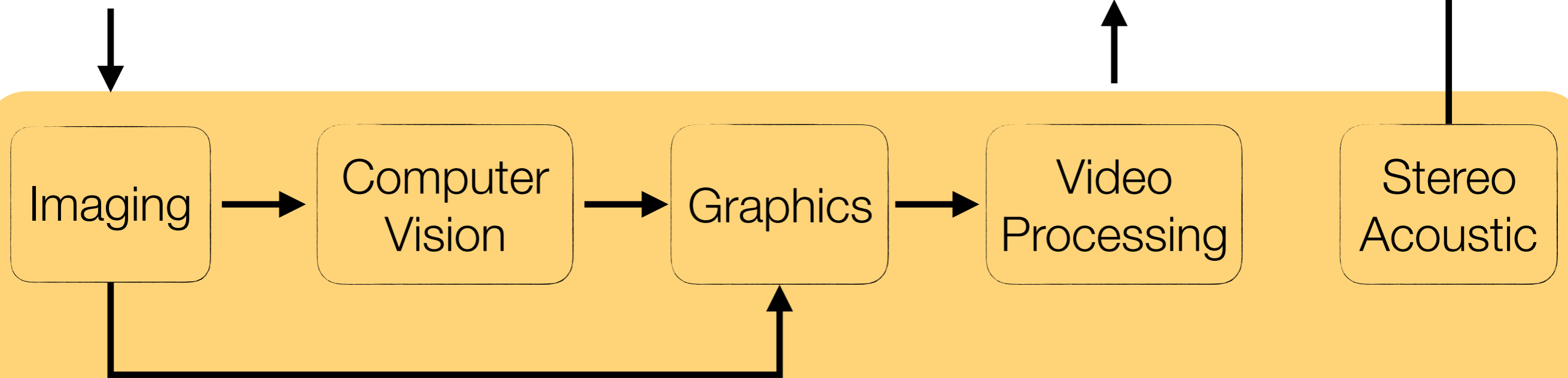


Emerging Applications Integrate All Components

Camera



Headset



**Co-Optimize/Design Different Computing Domains
Across the Entire SoC**

Emma Wang
@Harvard

GPU

GPU Shared
Logic

A3

CDI

FS

DDR

GPU

GPU

PLLS

DDR

HDMI

PLL

SRAM

CPU 2

CPU 2

CPU 2

SRAM

CPU 2

DDR

DDR

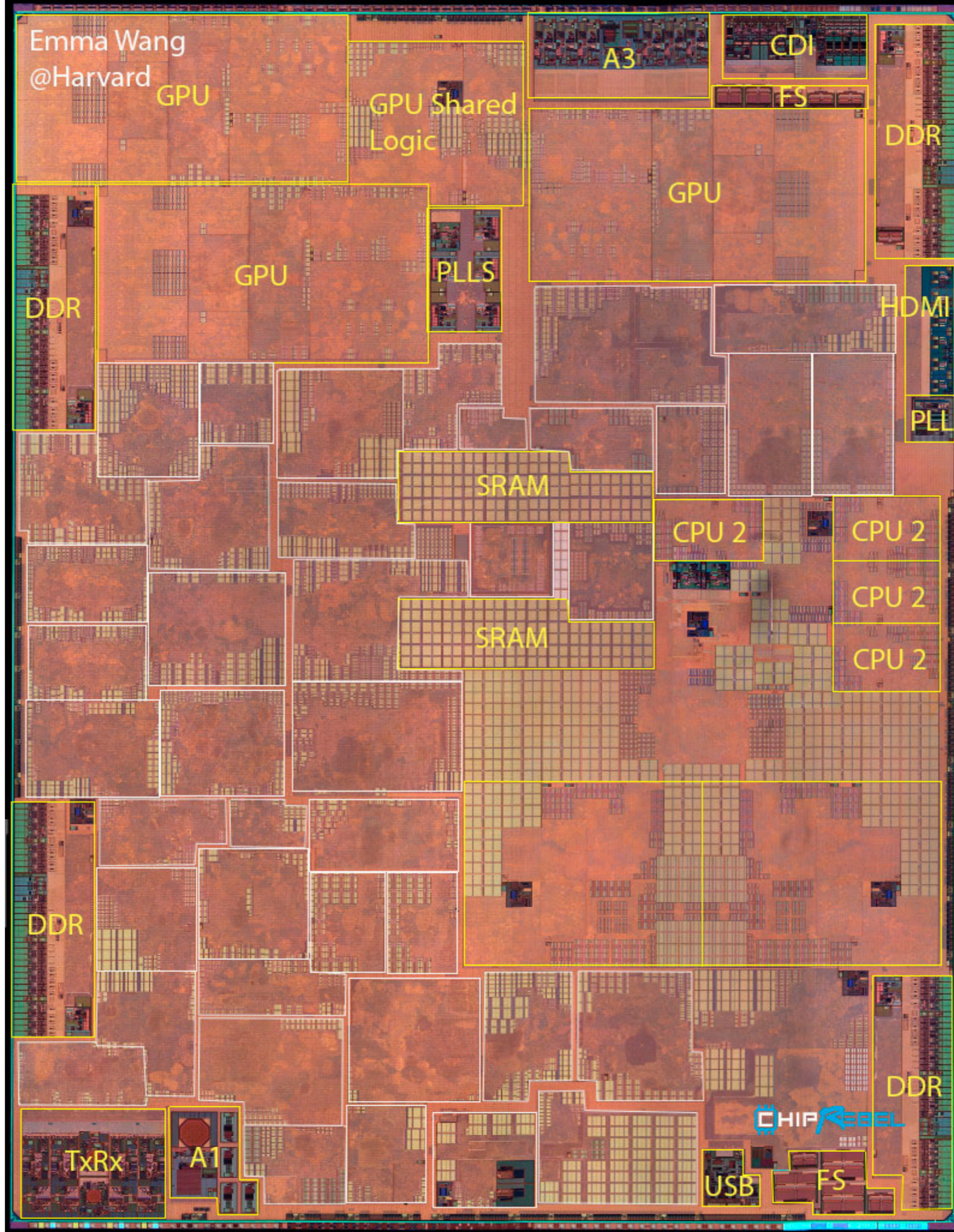
TxRx

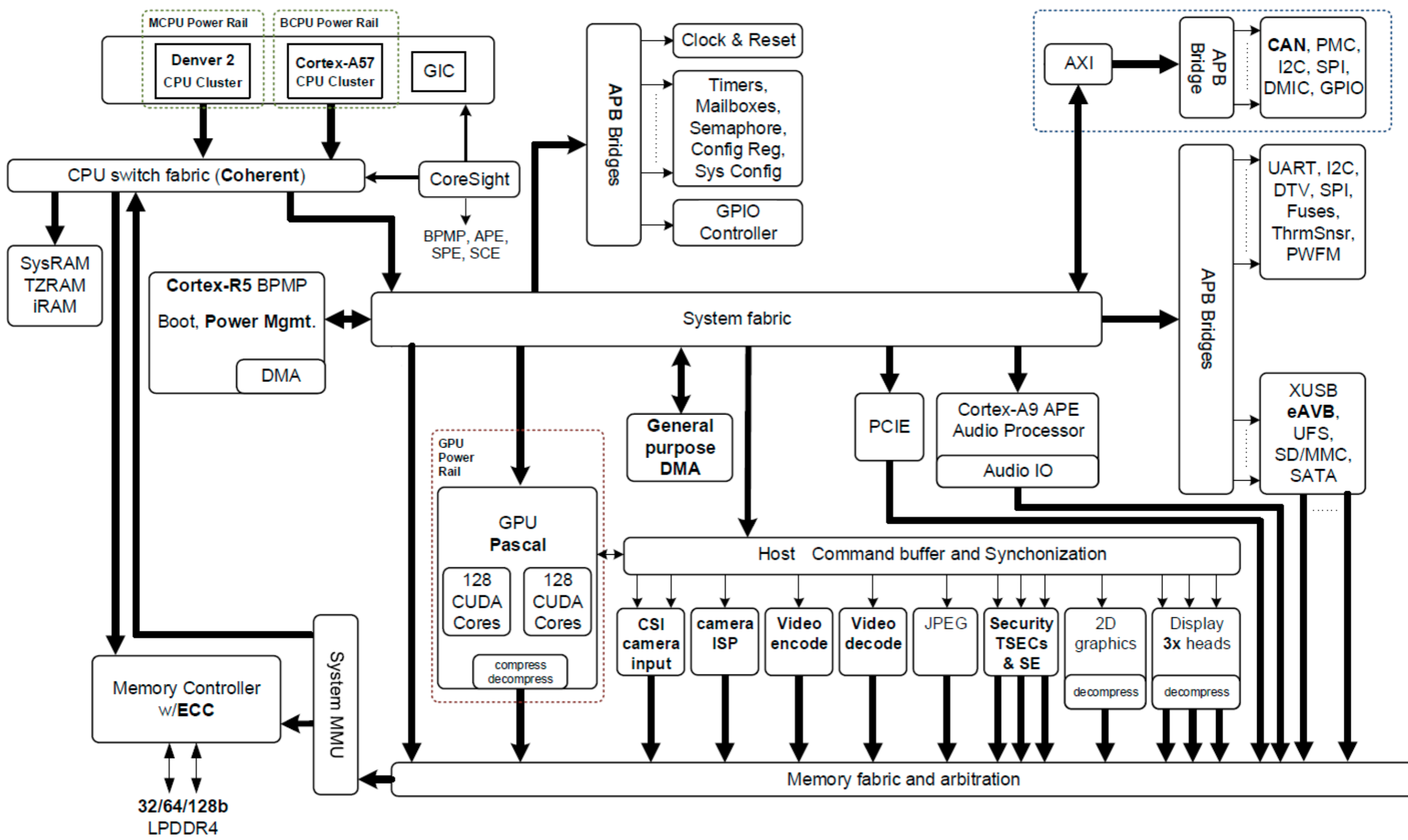
A1

CHIP REBEL

USB

FS





Nvidia TX2 SoC

You can't fix what you can't measure

Architecture Modeling Infrastructure

Target	Tool
CPU	Gem5/Marss86
GPU	GPGPUSim/GPUWattch
DRAM	DRAMSim2
DNN Accelerator	SCALESim/RTL
SoC	PARADE/GemDroid

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Why Do We Need Another SoC Modeling Tool?

Requirements for SoC-Level Modeling

- ▶ Do we need cycle-accurate CPU models in SoC Simulation?
- ▶ Do we need cycle-accurate GPU models in SoC Simulation?
- ▶ At what granularity should we model the SoC?
- ▶ What are evaluation metrics should we care about?
- ▶ What IP blocks should we support, and how do we support new IP blocks?
- ▶ First-order bottleneck analysis vs. detailed perf. model

Different Modeling Levels and Strategies

- ▶ Hardware Modeling

 - ▷ Analytical Model

 - ▷ Simulation Model

- ▶ Task-level Modeling

 - ▷ SoC-level tasks (case-study: continuous vision)

 - ▷ IP-level tasks (case-study: DNN accelerator)

Rest of the Agenda

- ▶ **Introduction and Welcome (Yuhao Zhu, Rochester)**
- ▶ Mobile Computing and SoC Analytical Modeling (VJ, Harvard)
- ▶ Platform Architecture Modeling Tutorial (Jun Qi, Synopsys)
- ▶ Platform Architecture Simulation Model of Gables (Xiaoyang Li, Synopsys)
- ▶ Task-level Modeling: A Continuous Vision Case-Study (Yiming Gan, Rochester)
- ▶ Joint Optimization of Hardware and Compiler -- Modeling AI Accelerators using Platform Architect (Xiaoyang Li, Synopsys)