

Evolving Image Sensor Architecture through Stacking Devices

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Short Biography



Yusuke Oike

joined Sony Corporation, after he received Ph.D. degree in electronic engineering from the University of Tokyo in 2005, where he has been involved in research and development of architectures, circuits and devices for image sensors. From 2010 to 2011, he was a visiting scholar at Stanford University. Currently, He is in charge of developing CMOS image sensors as Deputy Senior General Manager of Sony Semiconductor Solutions. He is also appointed as Distinguished Engineer of Sony Corporation. He is the Program Chair of VLSI Symposium on Circuits 2021.

Agenda

- Introduction of stacked CMOS image sensor
- Performance improvement accelerated using 3D configuration
- Advancing pixel circuitry by pixel-pitch Cu–Cu connections
- Possible architectures of pixel-parallel digitization
- Hybrid Integration stacked on Si readout circuitry
- Integrating more intelligent processor with sensor

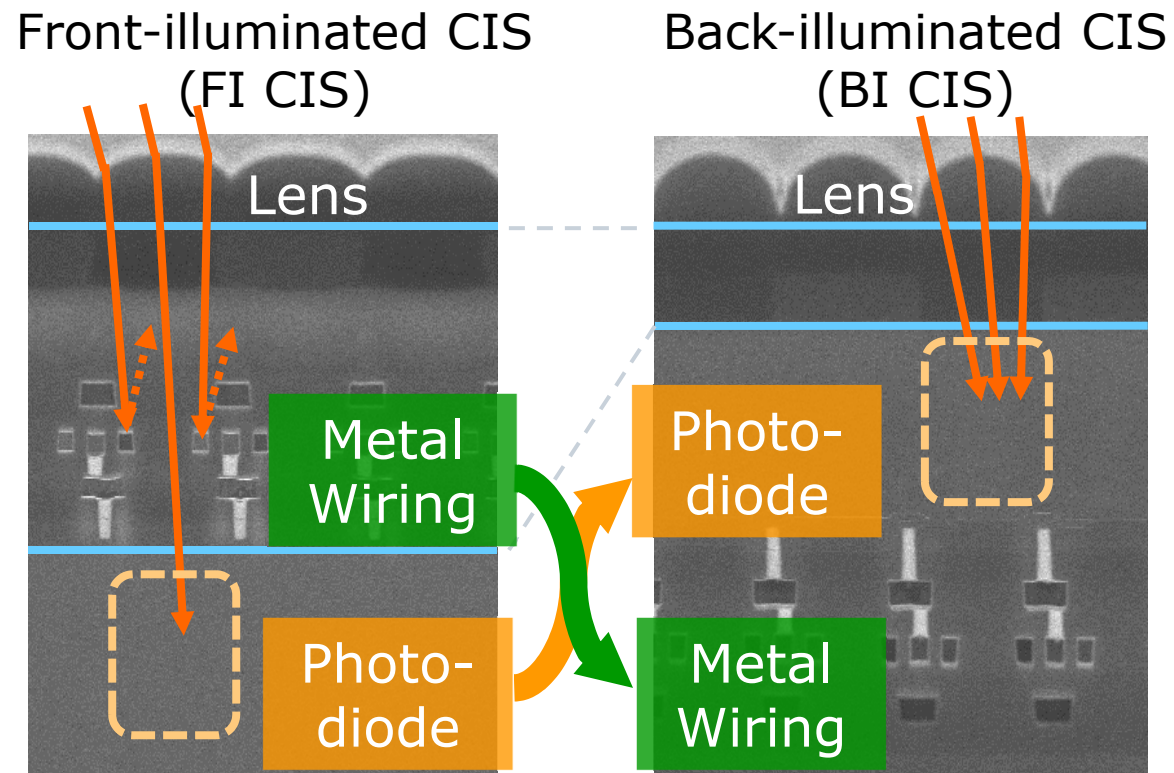
Image Sensor Applications

- Expanding to machine vision, network cameras and automotive applications

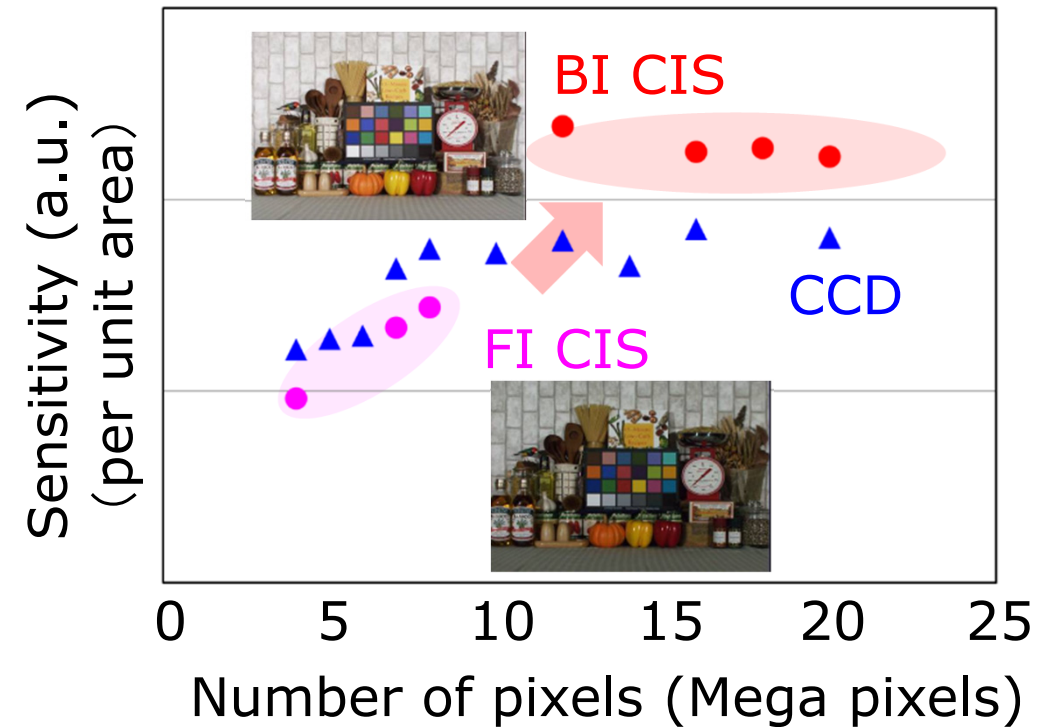


Back-illuminated CMOS Image Sensor

- Back-illuminated (BI) CMOS image sensor (CIS) has overcome drawback of sensitivity



S. Iwabuchi, ISSCC 2006

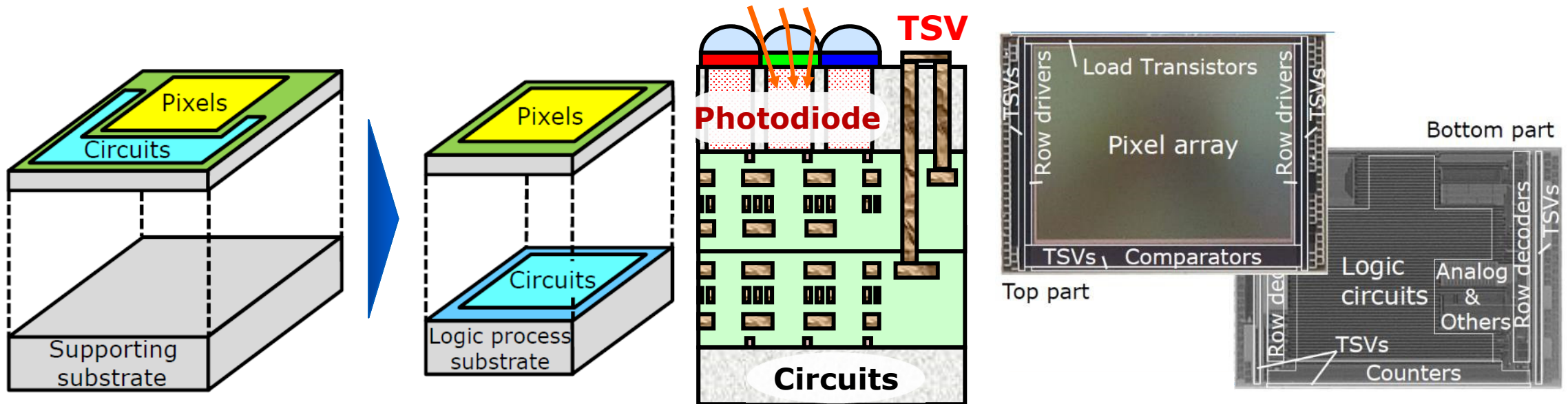


Stacked CMOS Image Sensor

- Stacked CIS has become mainstream in mobile cameras

Back-illuminated CIS

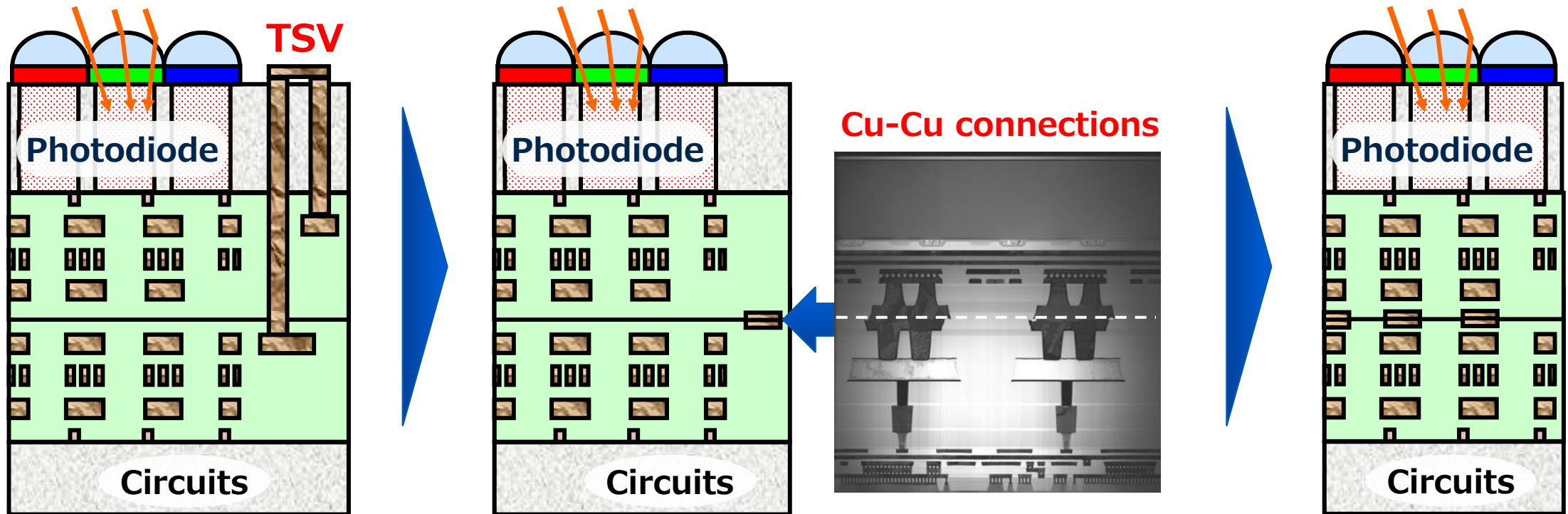
Stacked CIS



S. Sukegawa, ISSCC 2013

Cu-Cu Connections by Hybrid Bonding

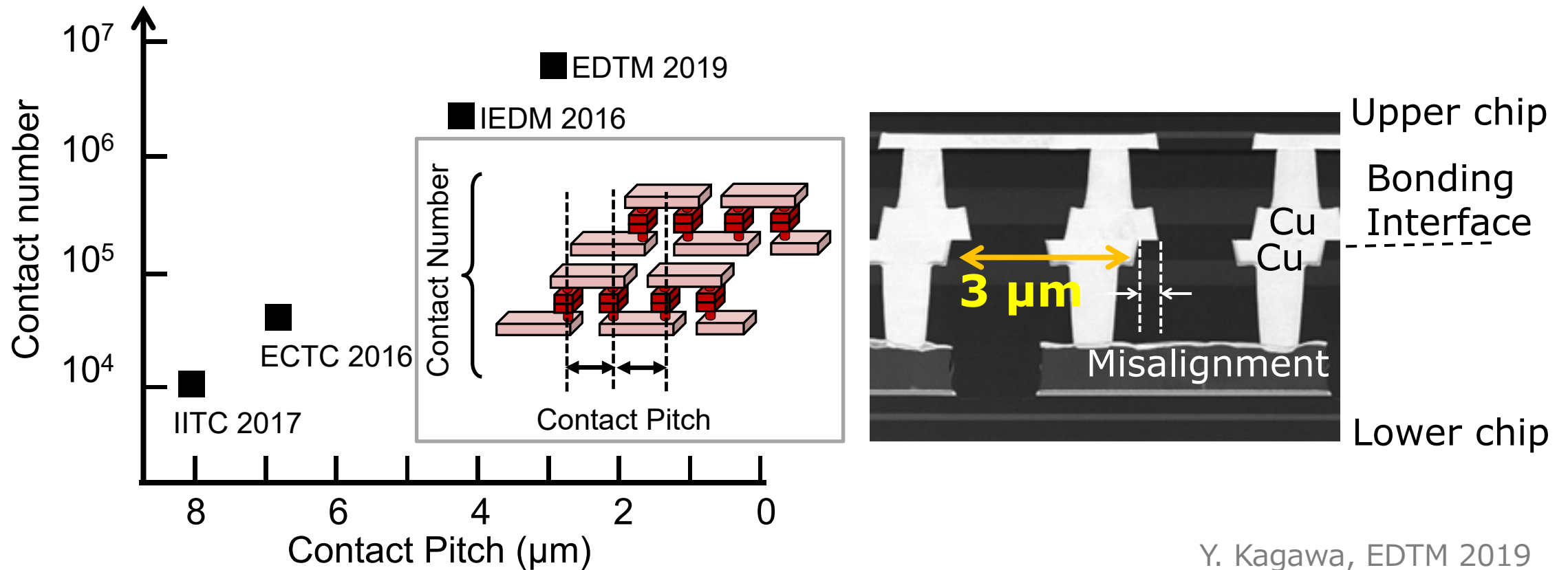
- Cu-Cu connections have been introduced under pixel arrays



Y. Kagawa, IEDM 2016

Trend of Cu-Cu Connection Pitch

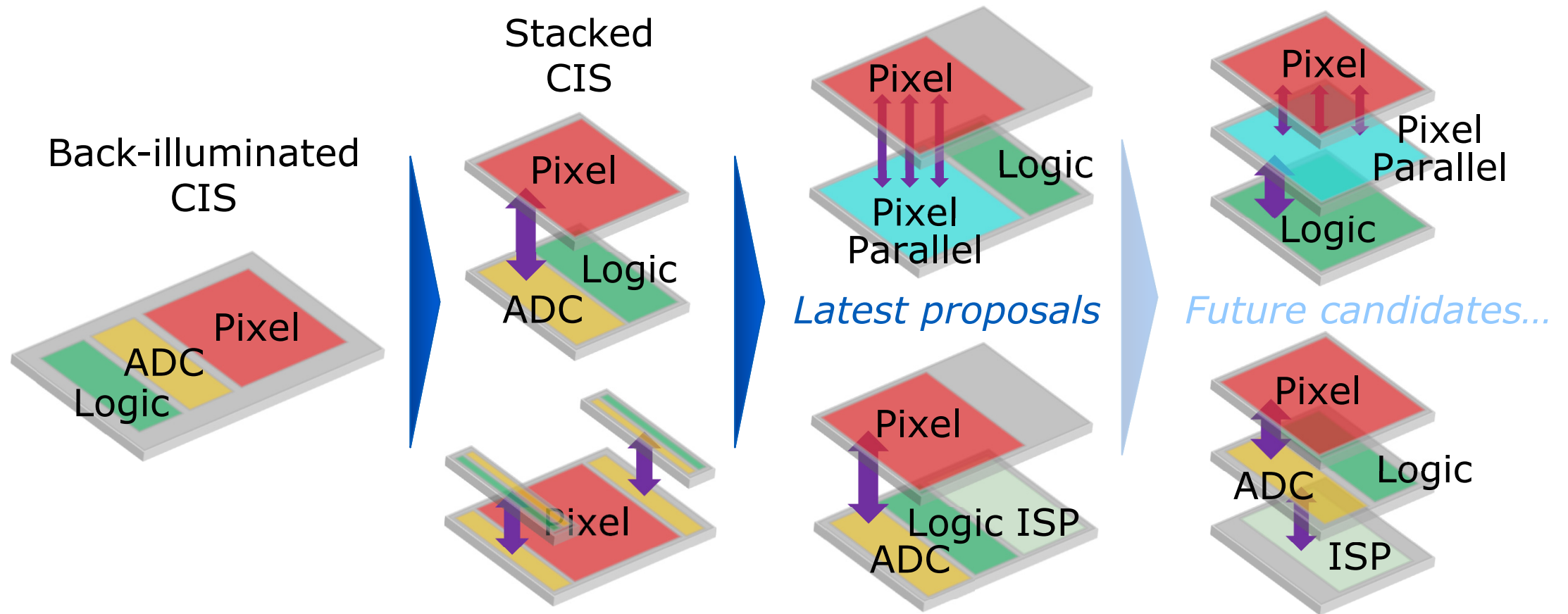
- Cu-Cu connection pitch is further being reduced to enable pixel-parallel architecture



Y. Kagawa, EDTM 2019

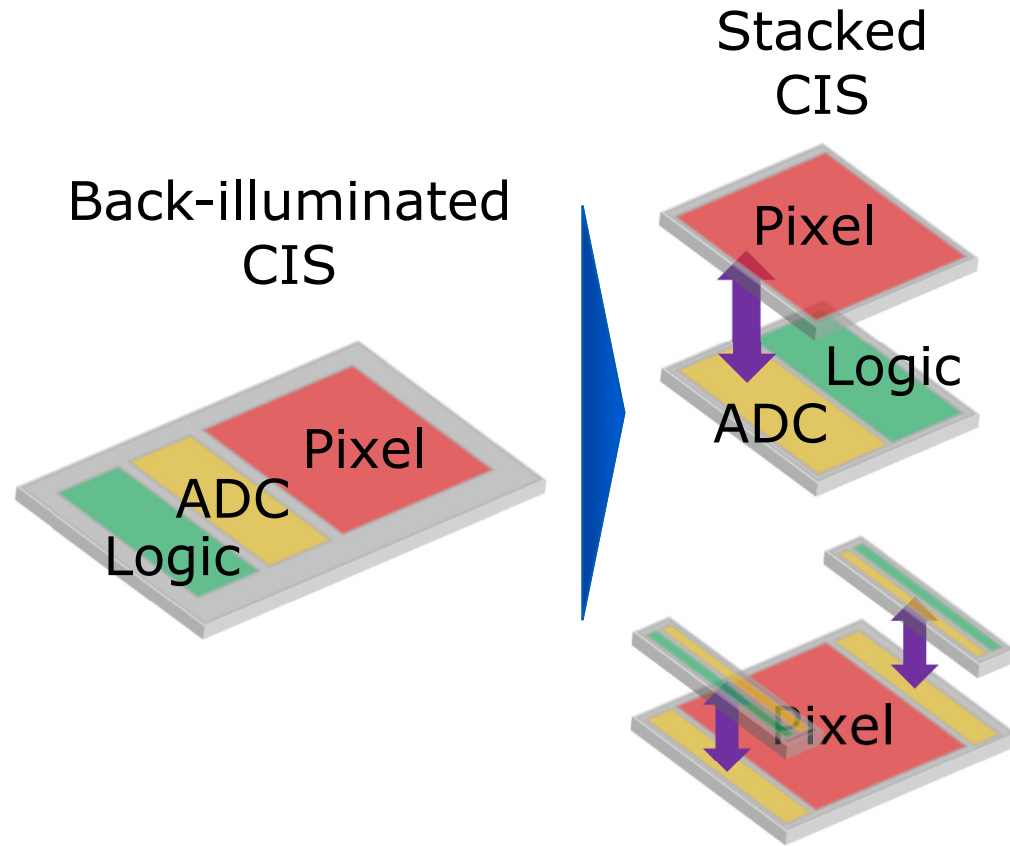
Prospect of Imaging Device using 3D Technologies

- Sensor architecture is evolving using 3D technologies



Stacked CMOS Image Sensor

- Performance improvement accelerated using 3D configuration

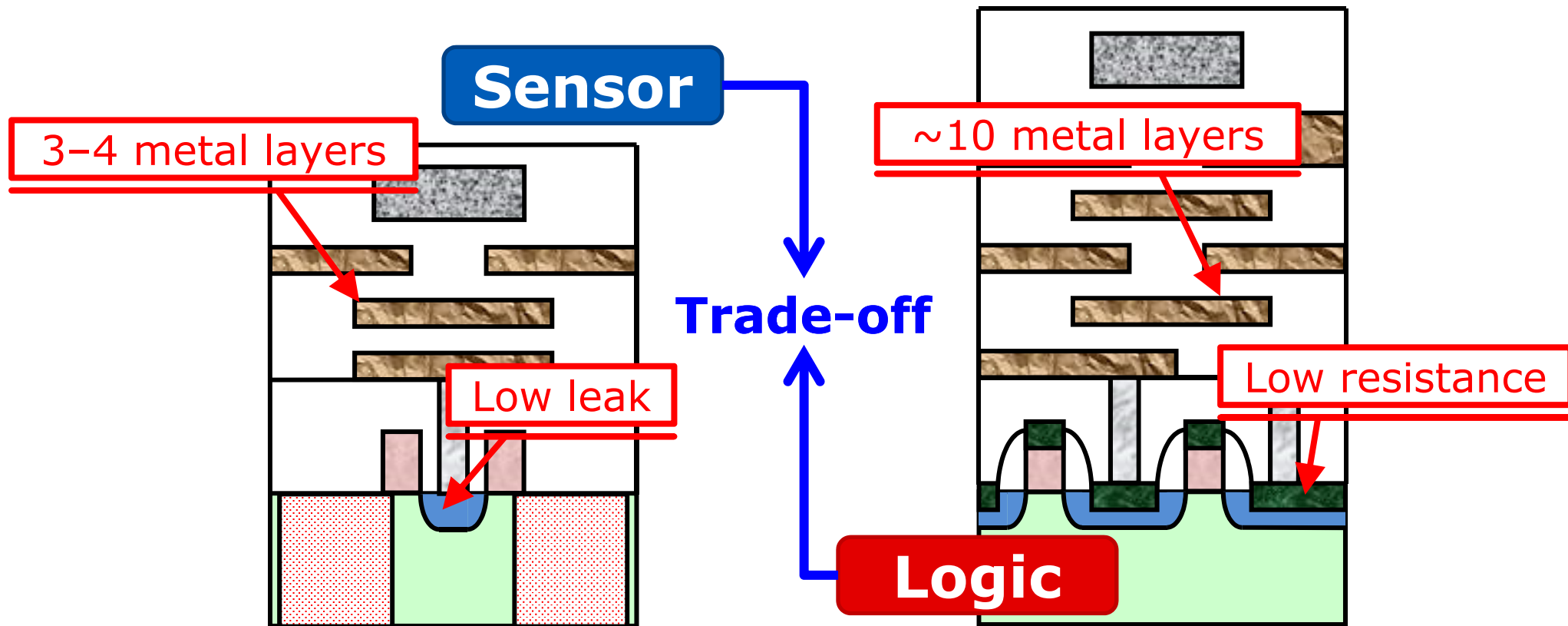


Highly parallel ADCs & Optimized process technologies

- Double parallel ADCs
- Chip-on-chip stacked CIS
- Three-layer stacked CIS

Trade-off Between Sensor and Logic Process

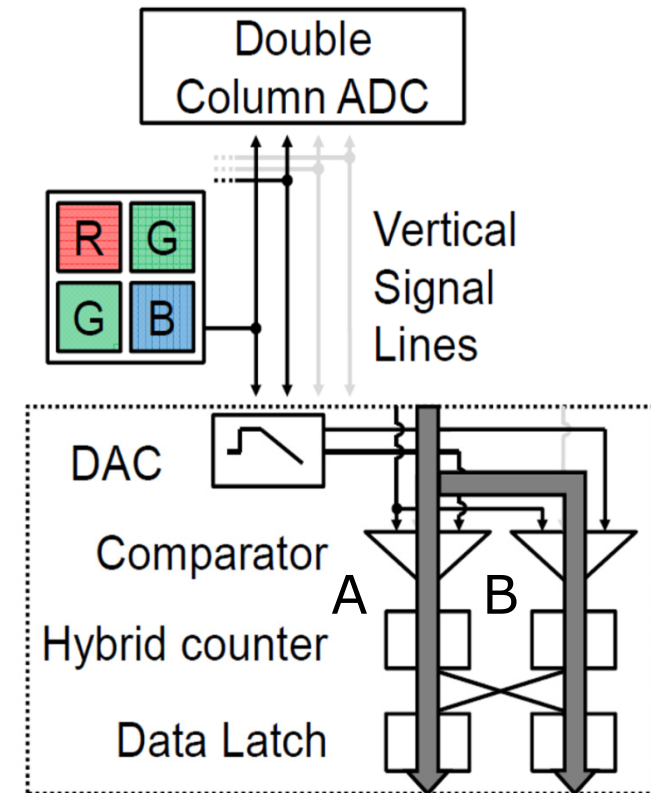
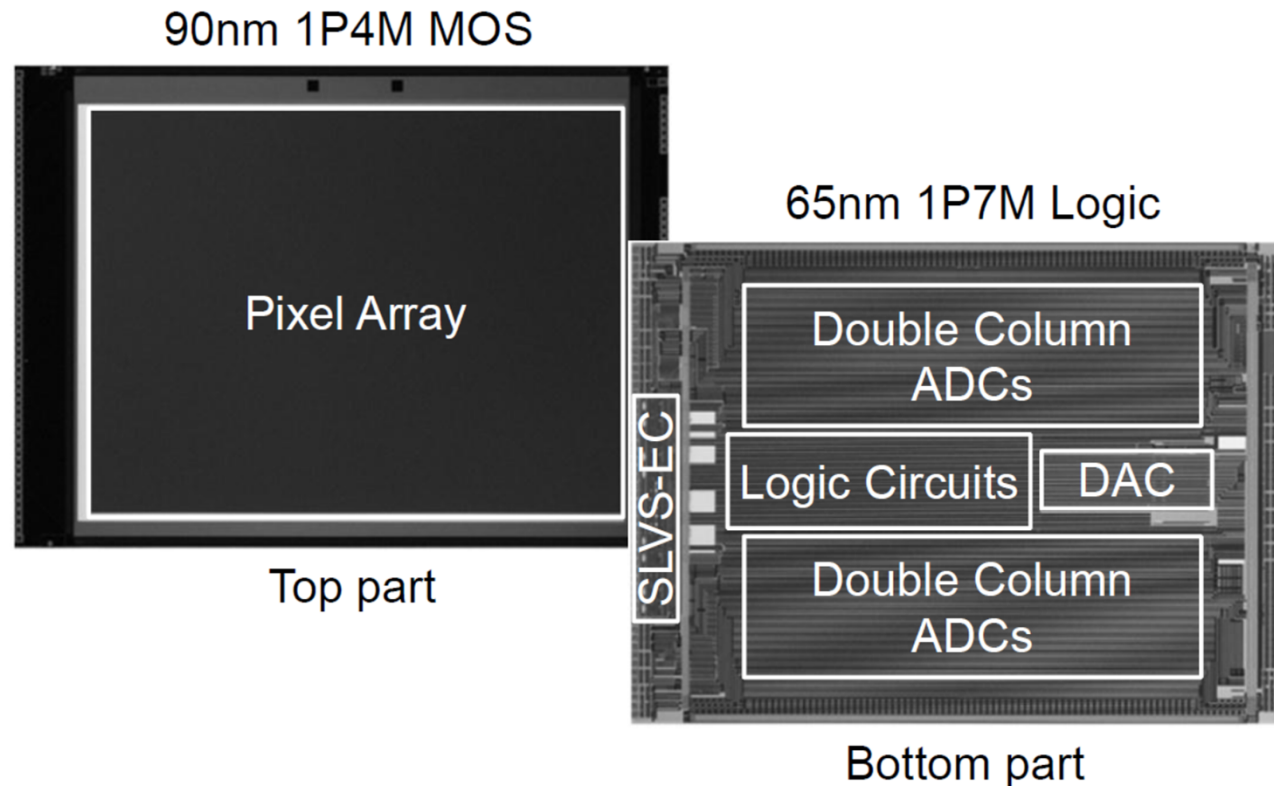
- Optimal process technologies differ based on sensor and logic; therefore, 3D stacking technology can relax this constraint



Performance Improvement by 3D Stacking

- Double column ADC integration achieves higher frame rates

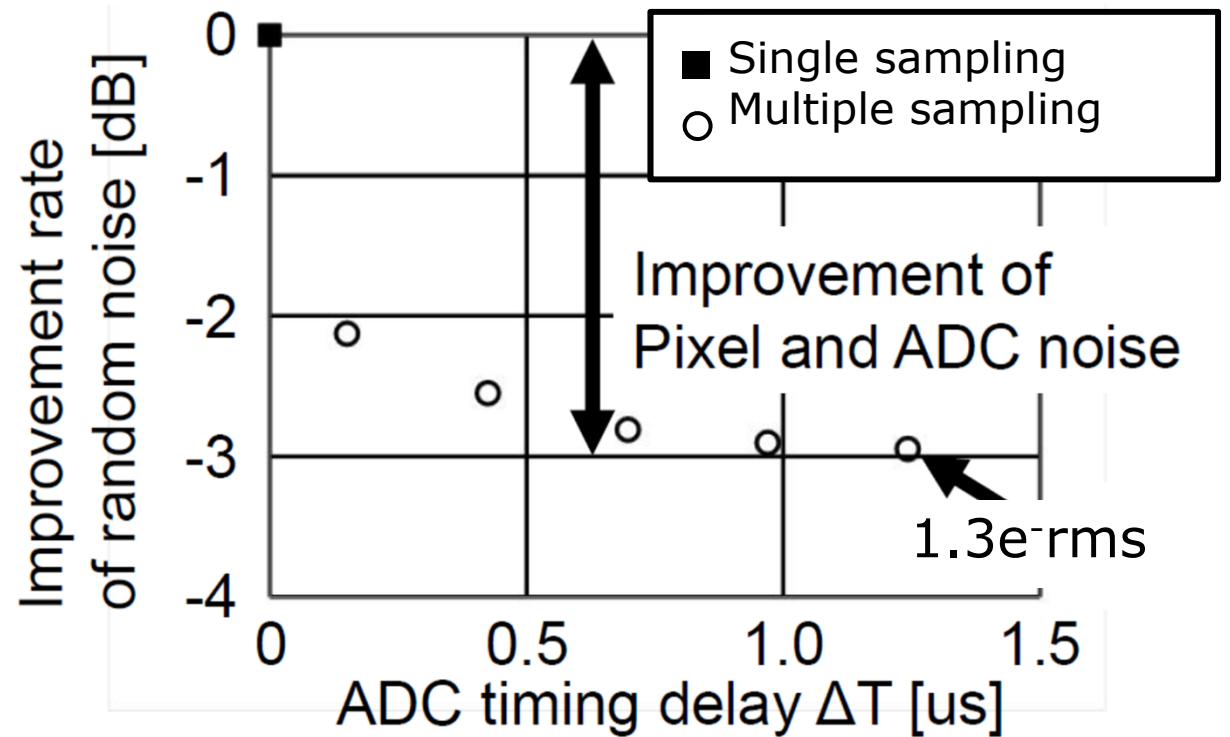
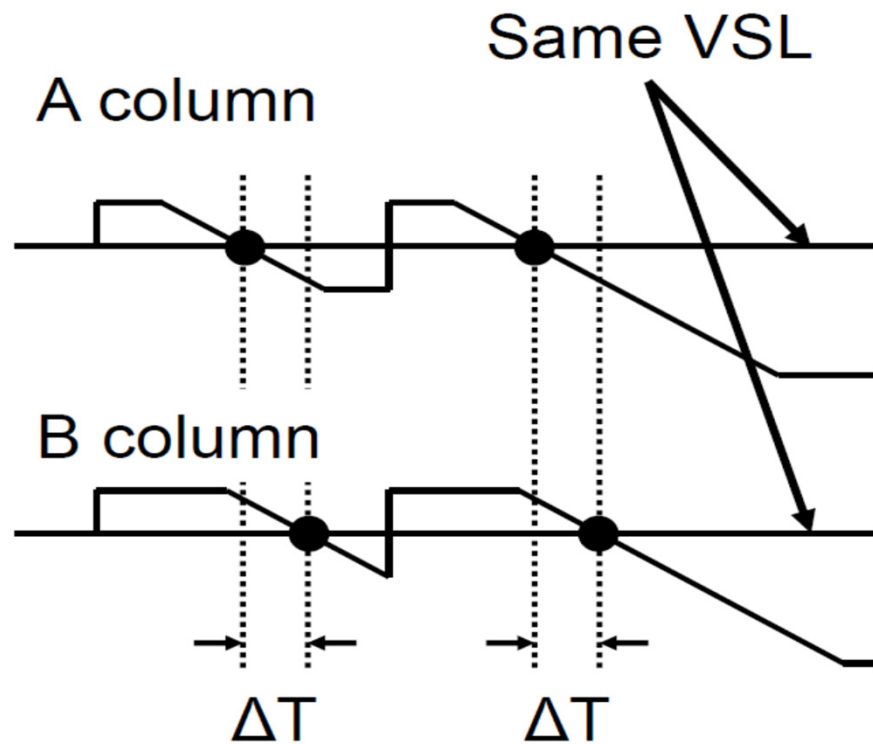
120 fps of 16M pixels



A. Suzuki, ISSCC 2015

Performance Improvement by 3D Stacking

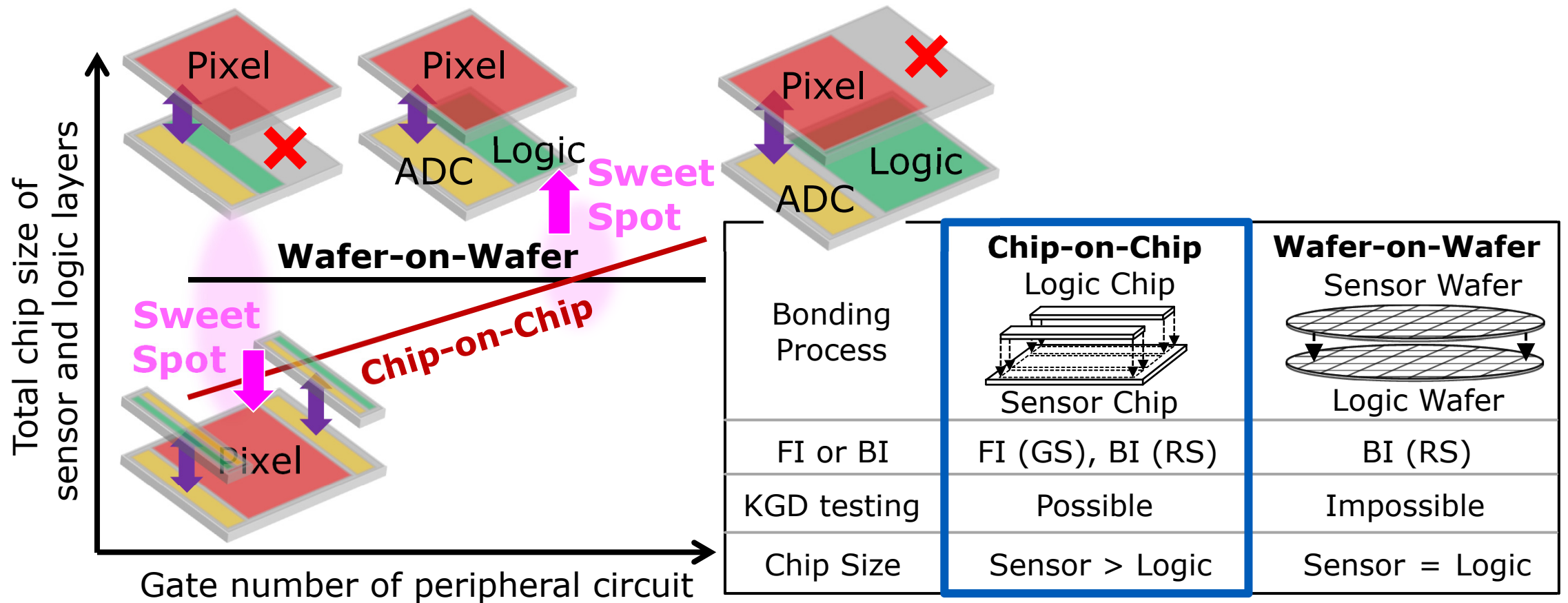
- Double column ADC integration also contributes low noise



A. Suzuki, ISSCC 2015

Chip-on-Chip 3D Integration

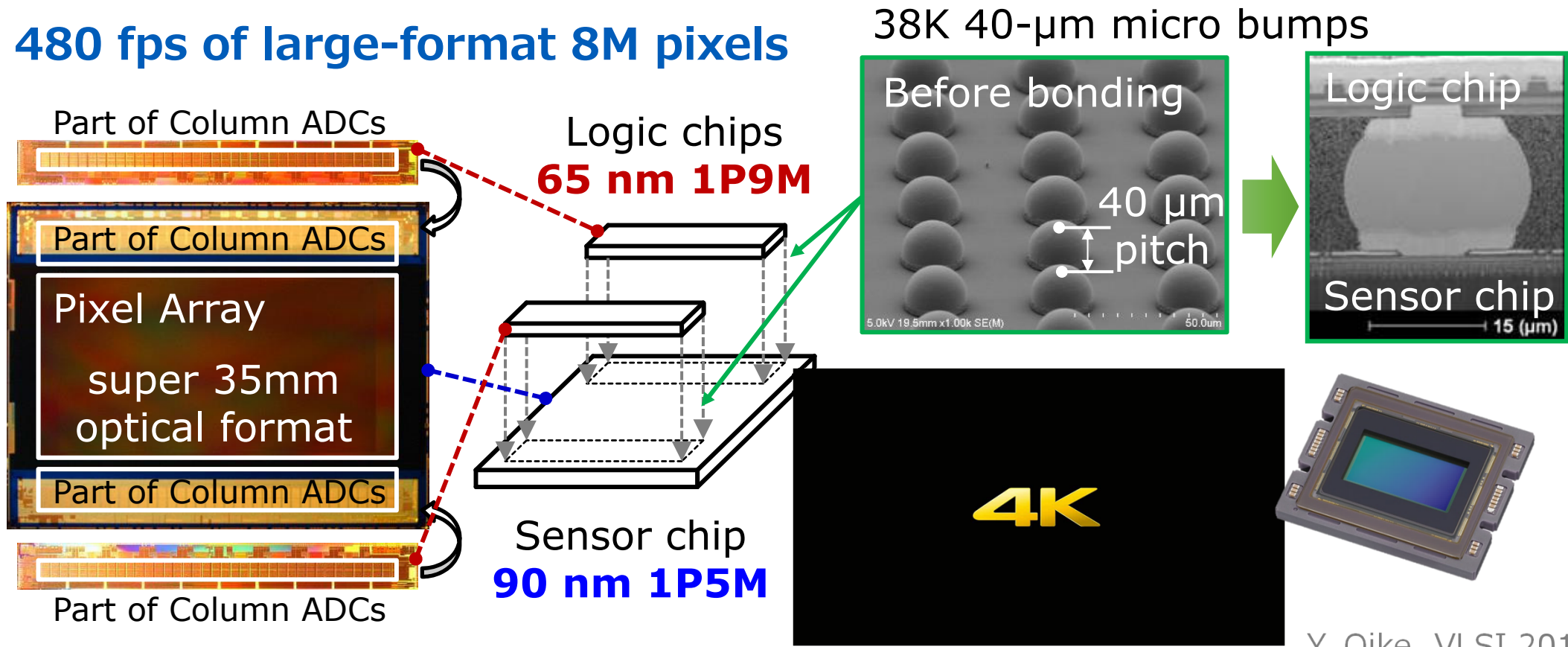
- Increase in area efficiency with large optical-format sensor



Chip-on-Chip 3D Integration

- 4K super slow motion realized in large optical format with CoC

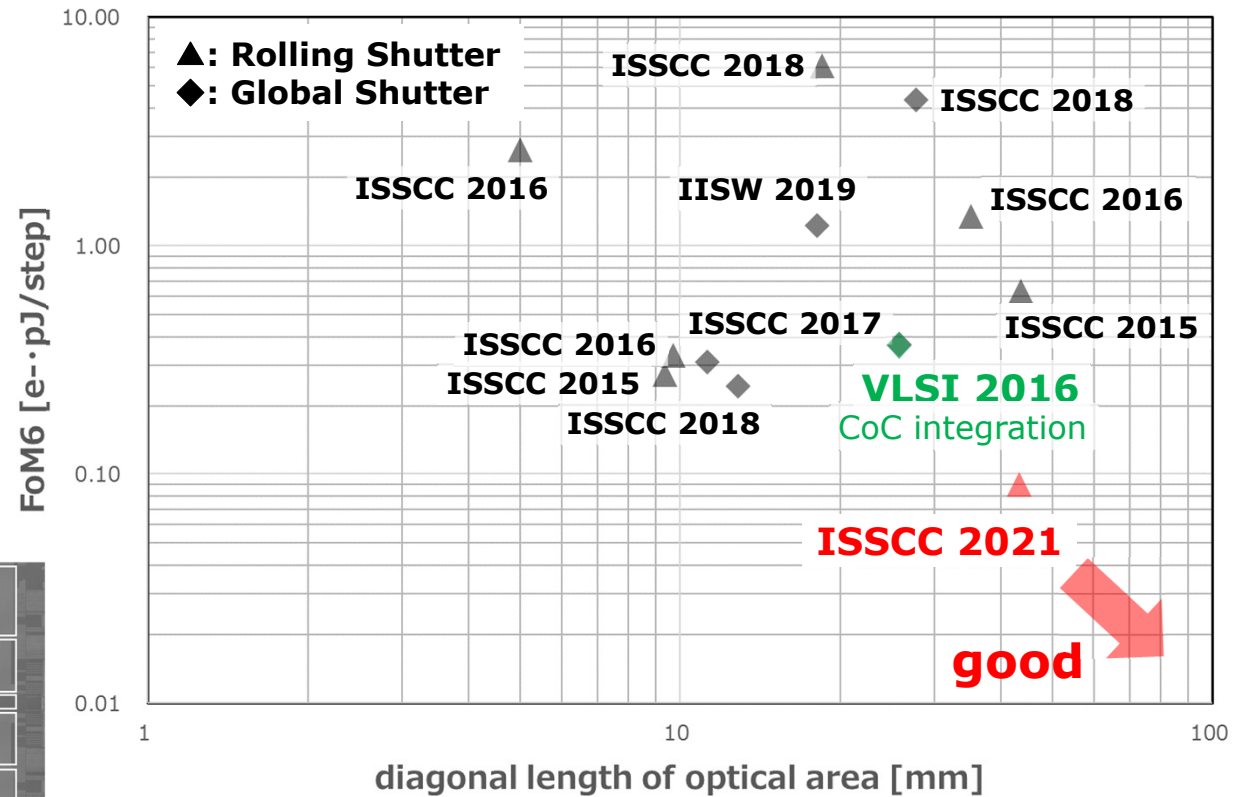
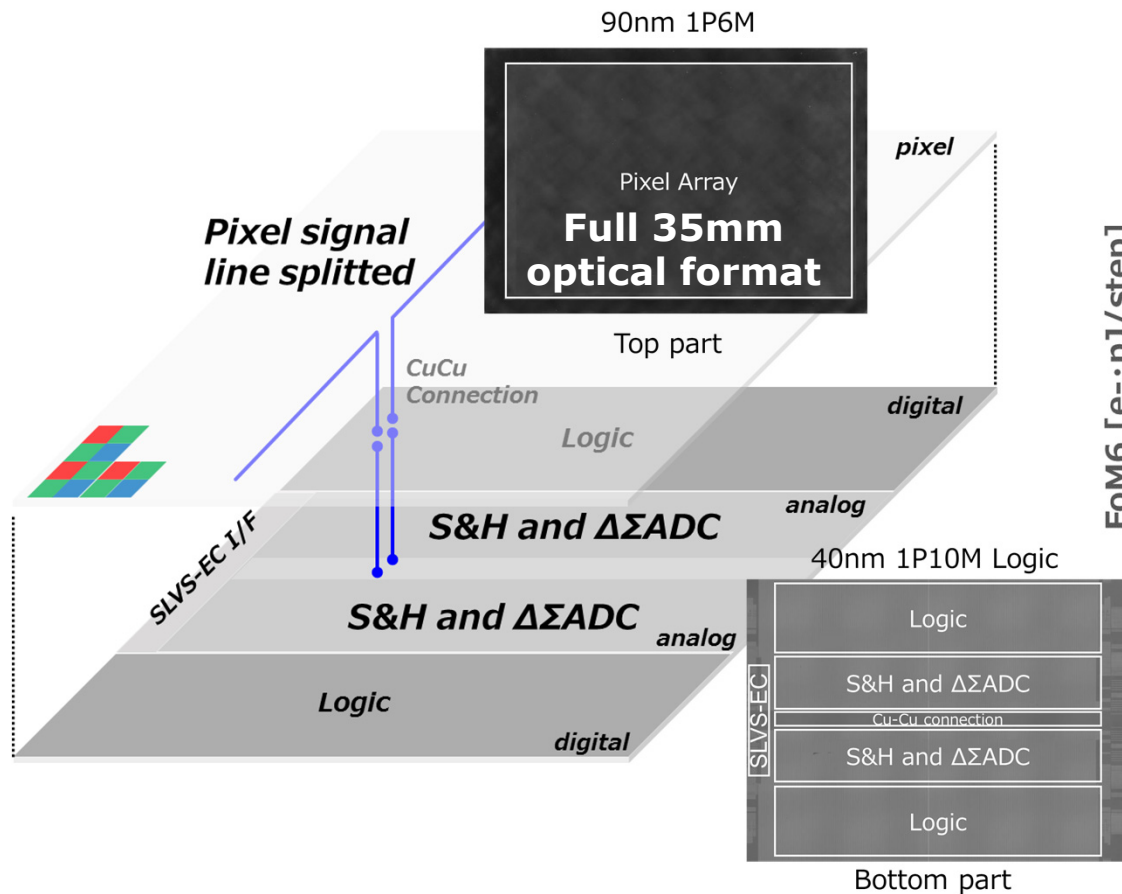
480 fps of large-format 8M pixels



Y. Oike, VLSI 2016

Latest Achievement in Large Optical Format

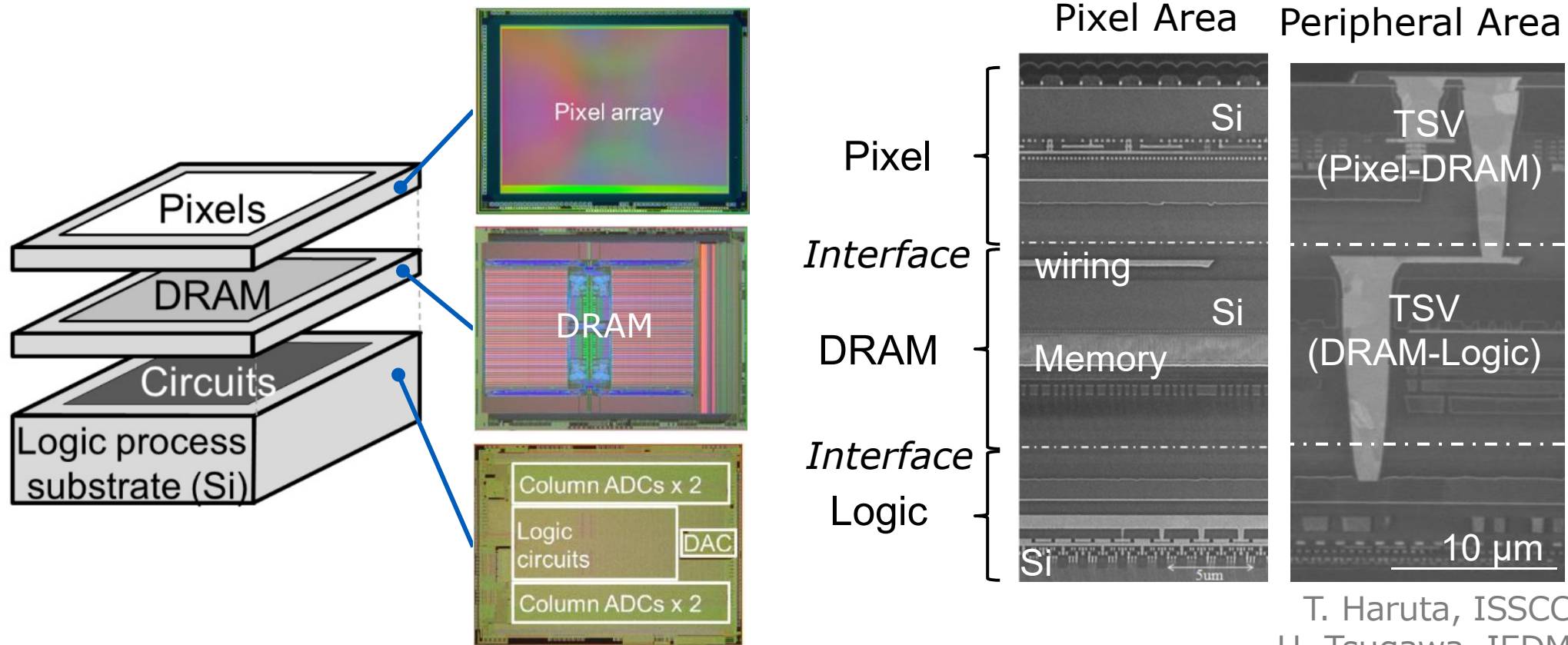
- 250 fps of 50M pixels in full 35-mm format achieved



To be presented by C. Okada, ISSCC 2021

Three-layer Stacked CIS with DRAM

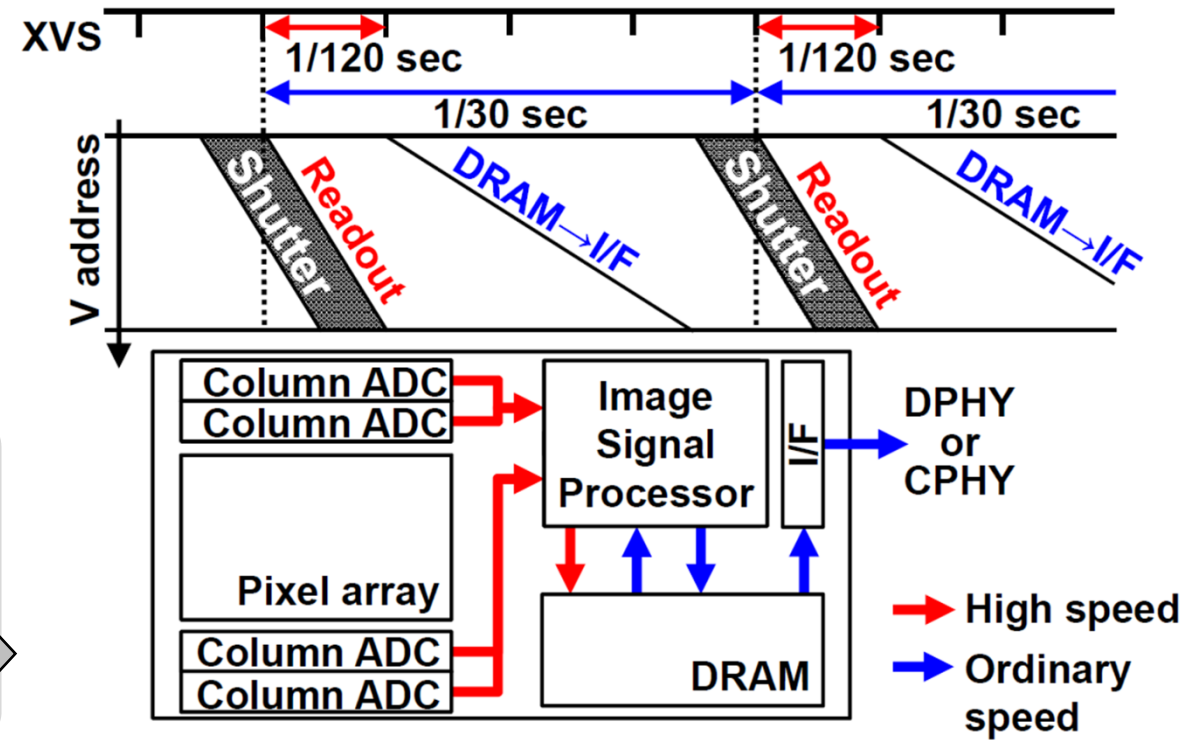
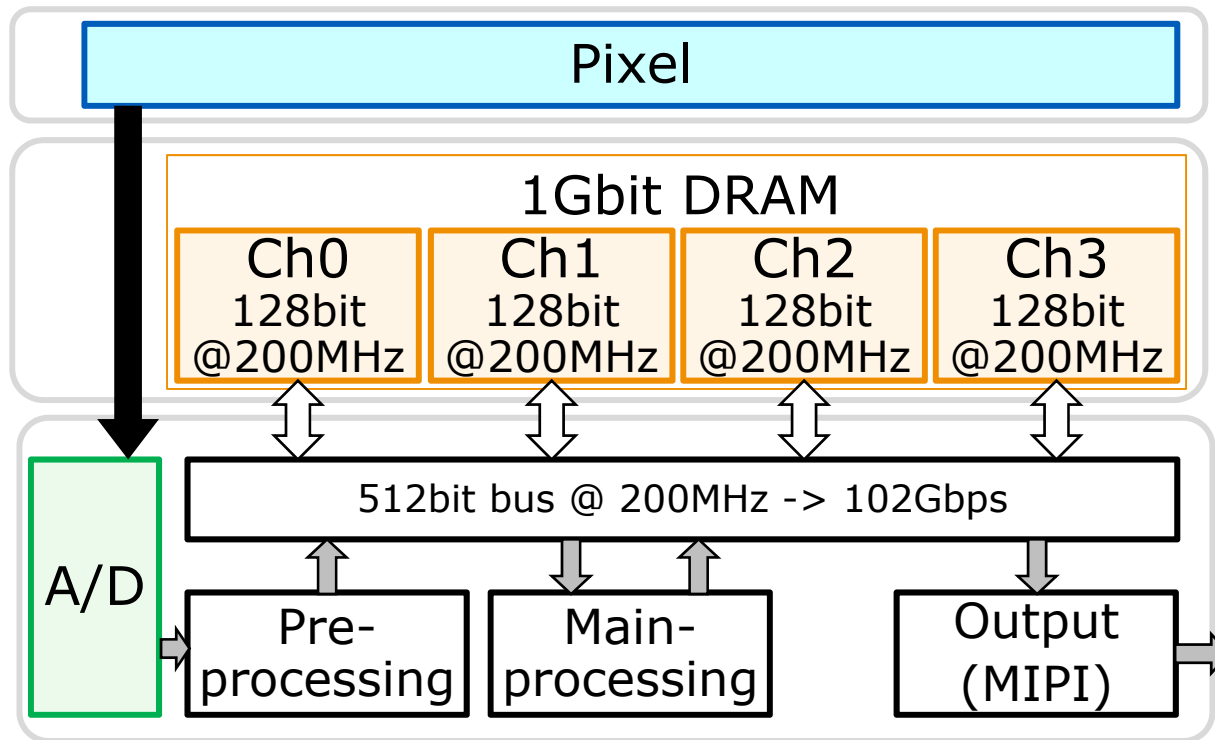
- DRAM buffer having wide data bandwidth for slow-motion capture



T. Haruta, ISSCC 2017
H. Tsugawa, IEDM 2017

Three-layer Stacked CIS with DRAM

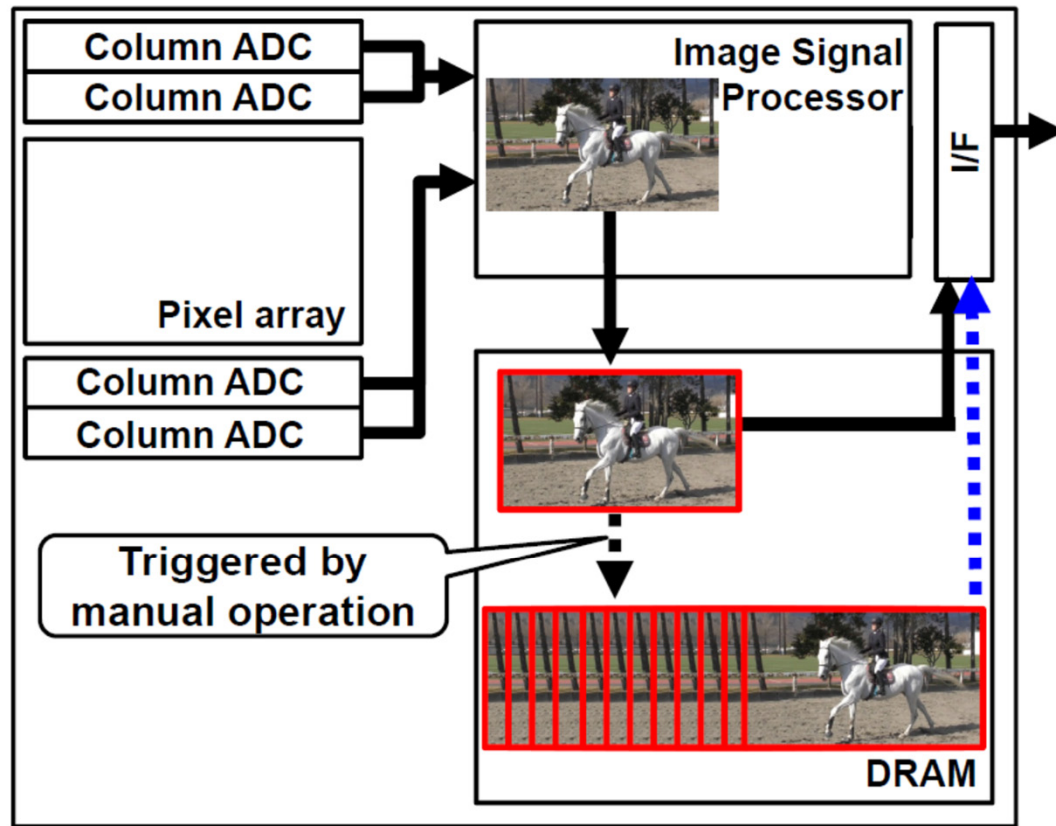
- Enables slow-motion capture overcoming I/F limitation



T. Haruta, ISSCC 2017

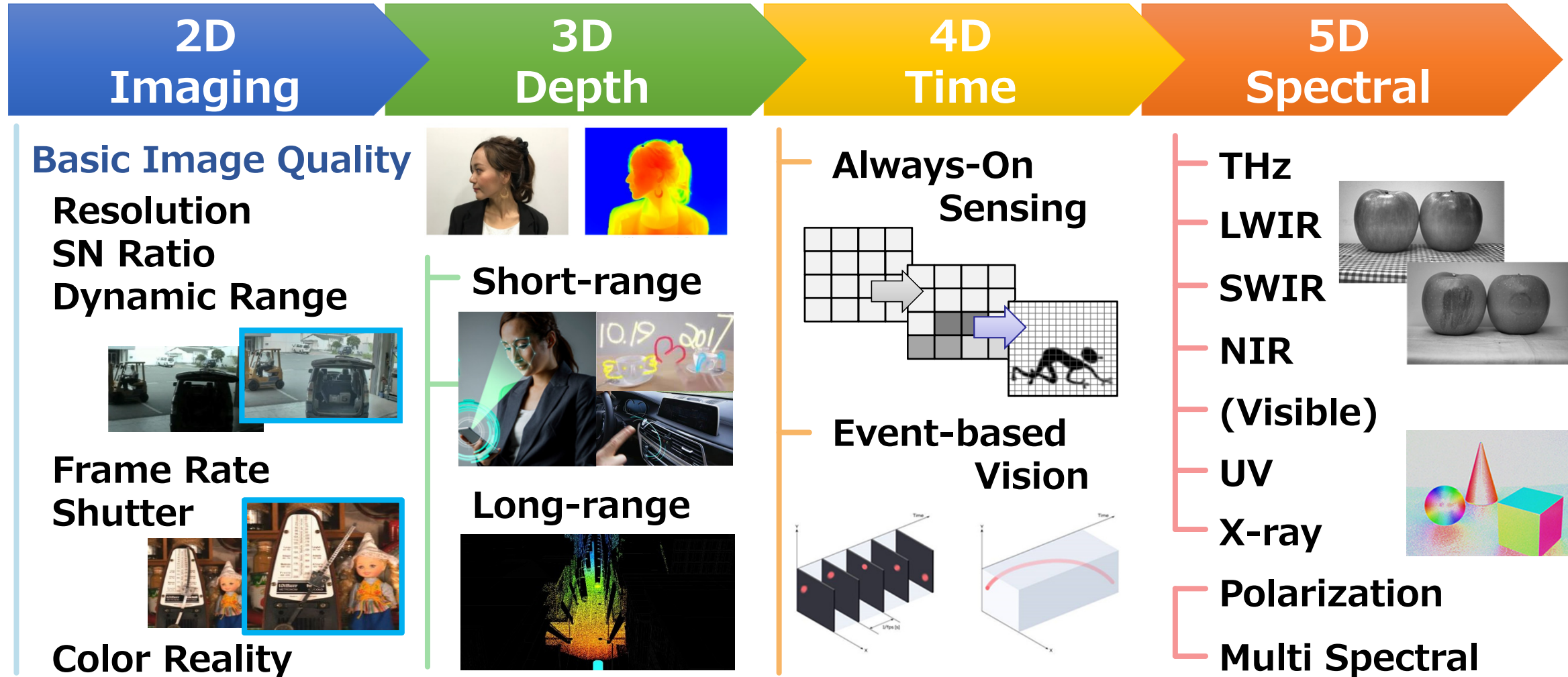
Three-layer Stacked CIS with DRAM

- 960-fps slow-motion capture buffered in stacked DRAM



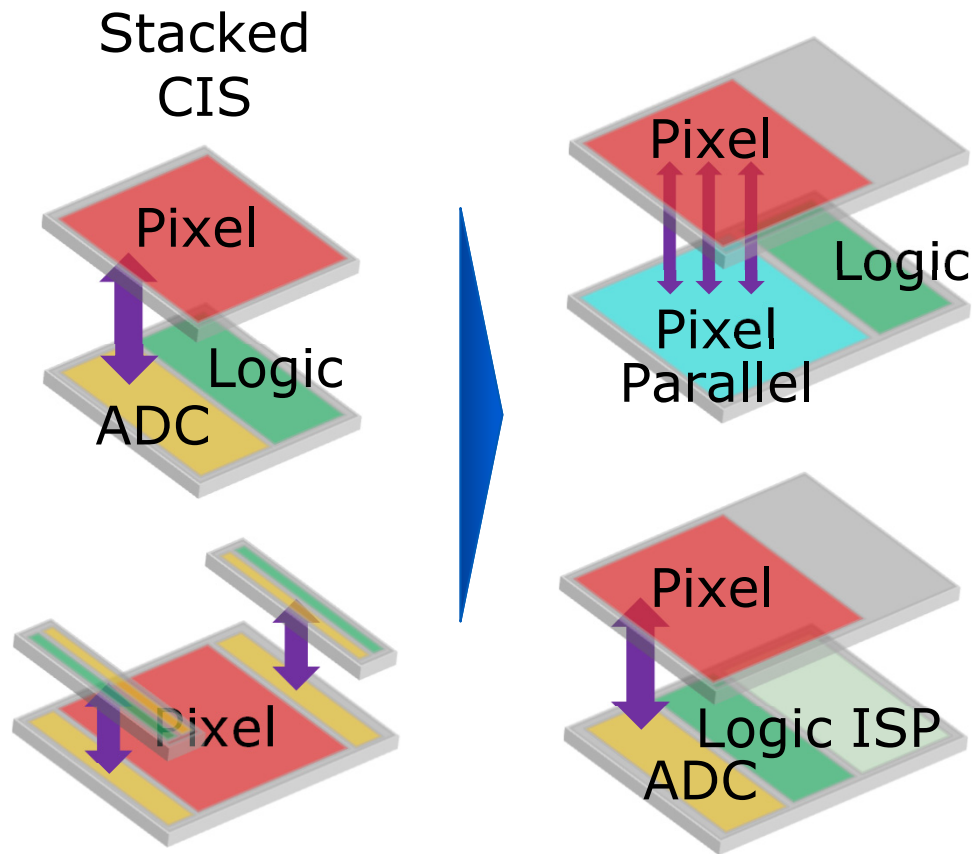
T. Haruta, ISSCC 2017

Expanding Sensing Functionalities



Advanced Architectures Using 3D Technologies

- Sensor architecture is evolving using 3D technologies



More advanced pixel circuitry

- Stacked pixel circuitry
- Event-based vision sensing
- Pixel-parallel ADC architecture
- SPAD-based photon counting

Hybrid Integration on Si

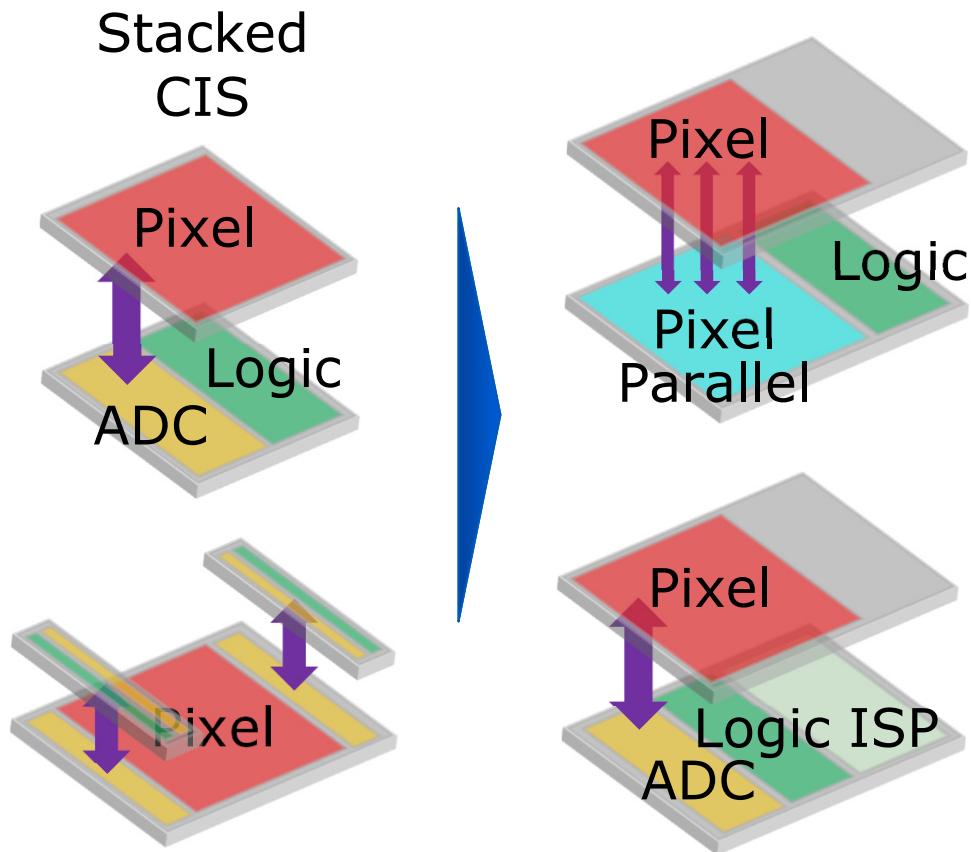
- SWIR InGaAs photodetector

Integrating more intelligent processor with sensor

- Intelligent vision sensor

More Advanced Pixel Circuitry

- Sensor architecture is evolving using 3D technologies



More advanced pixel circuitry

- Stacked pixel circuitry
- Event-based vision sensing
- Pixel-parallel ADC architecture
- SPAD-based photon counting

Hybrid Integration on Si

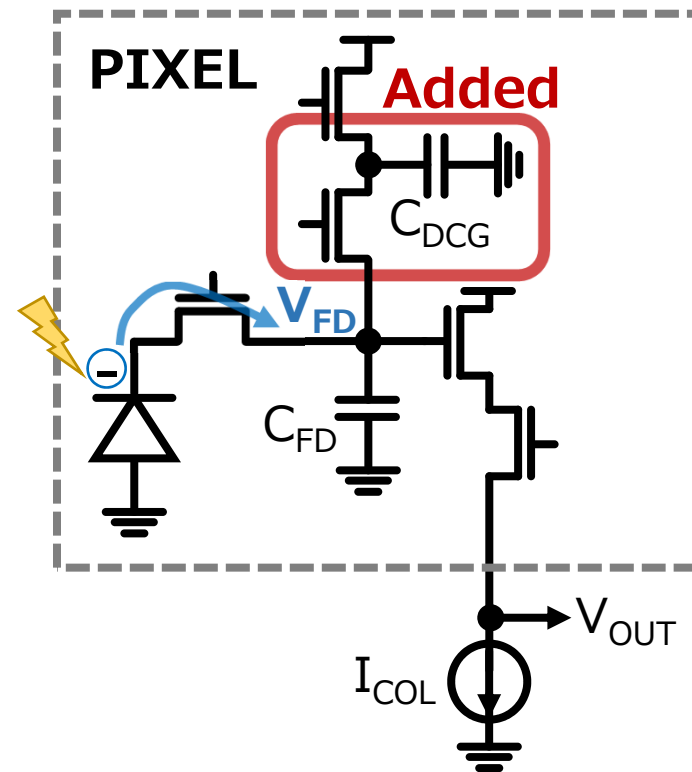
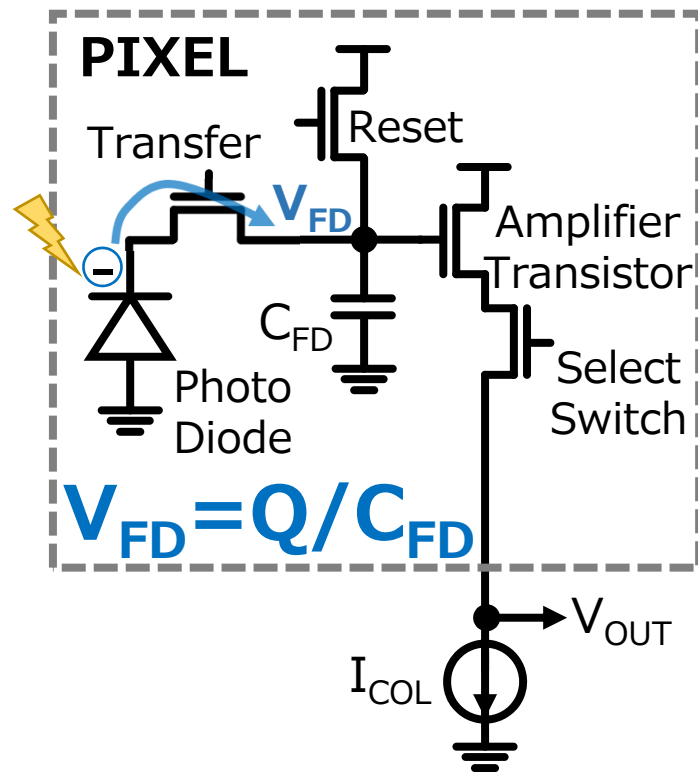
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Integrating more intelligent processor with sensor

- Intelligent vision sensor

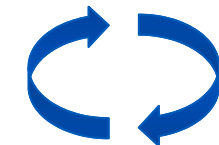
Dual Conversion Gain Pixel for HDR

- Dual conversion gain (DCG) pixel is a technique to ensure both low noise and high dynamic range but requires additional circuitry



$$V_{FD} = Q / C_{FD}$$

Low Noise

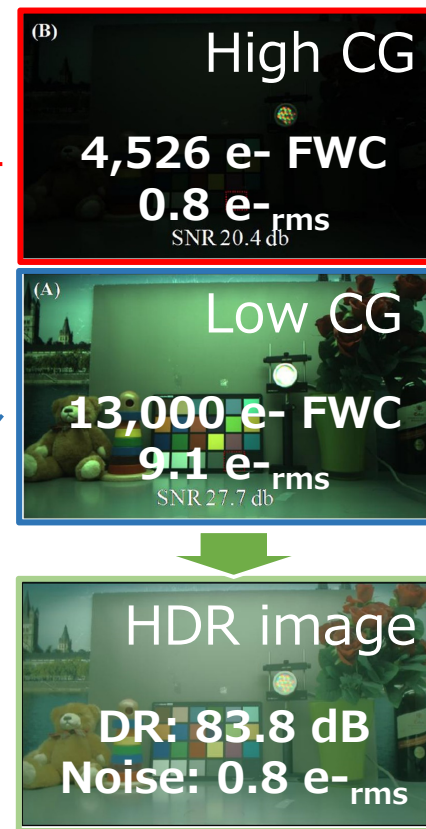
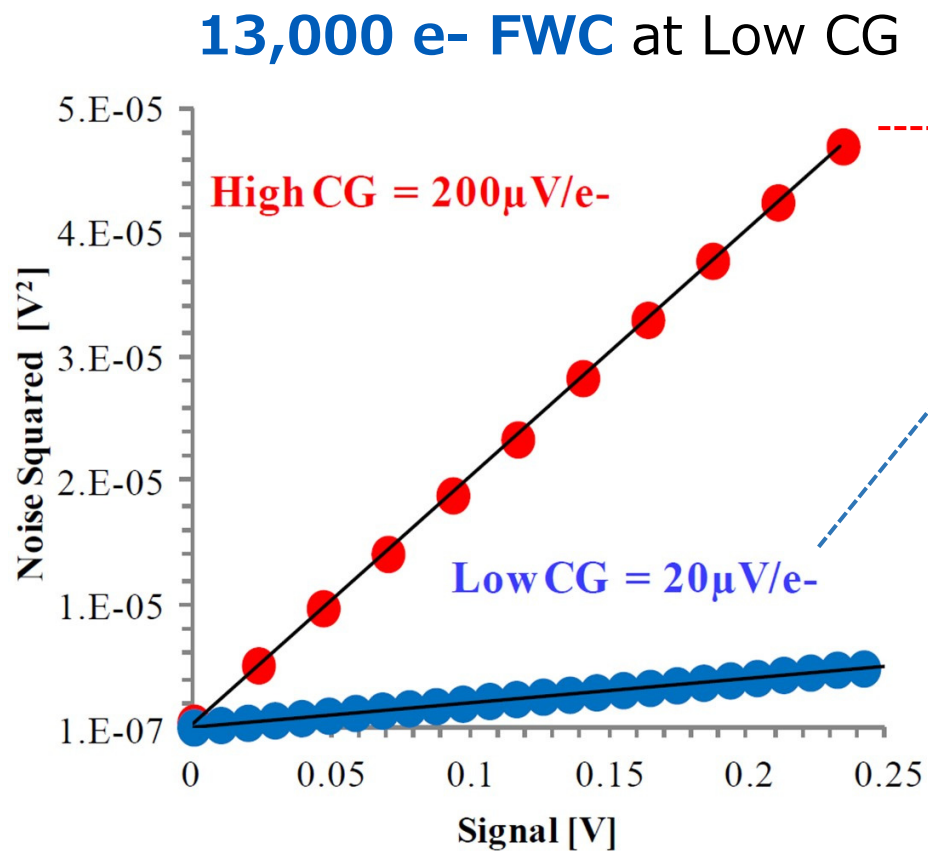
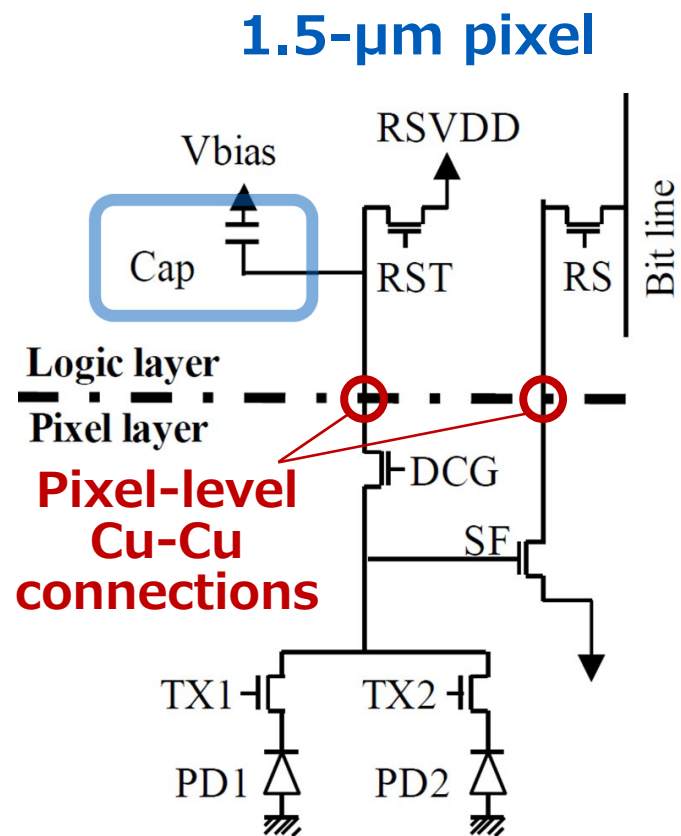


$$V_{FD} = Q / (C_{FD} + C_{DCG})$$

High Capacity for HDR

Dual Conversion Gain Pixel with Stacked Circuitry

- Stacked pixel circuitry enables reducing DCG pixel with high FWC

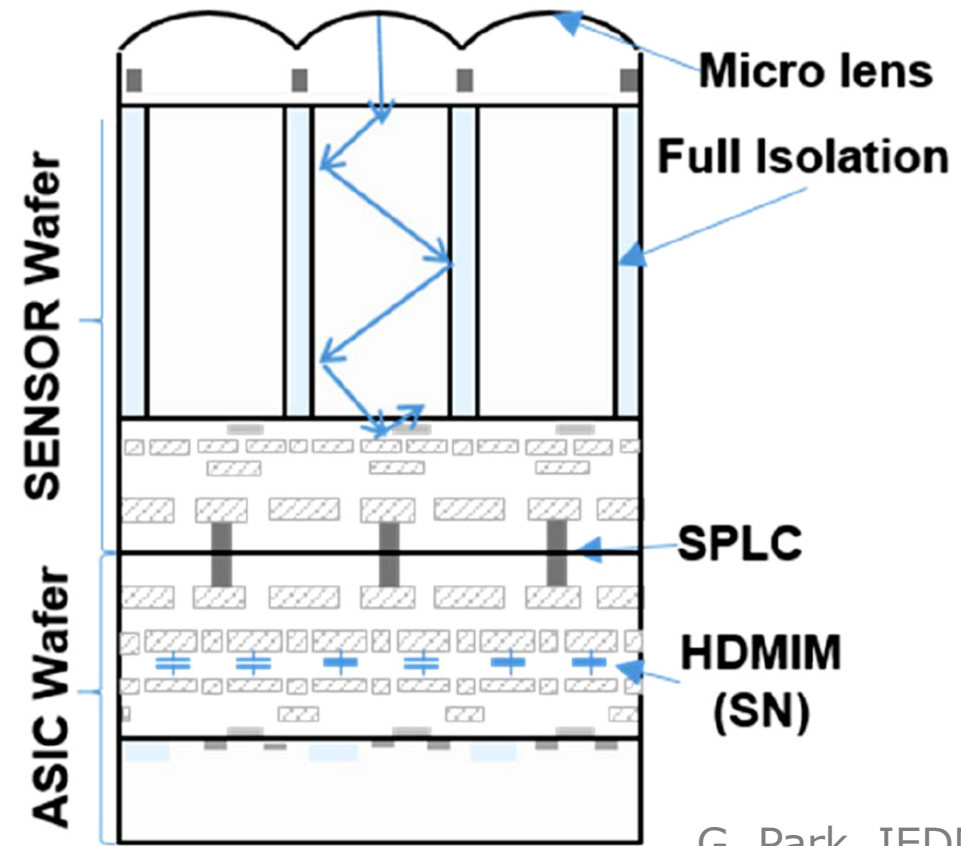
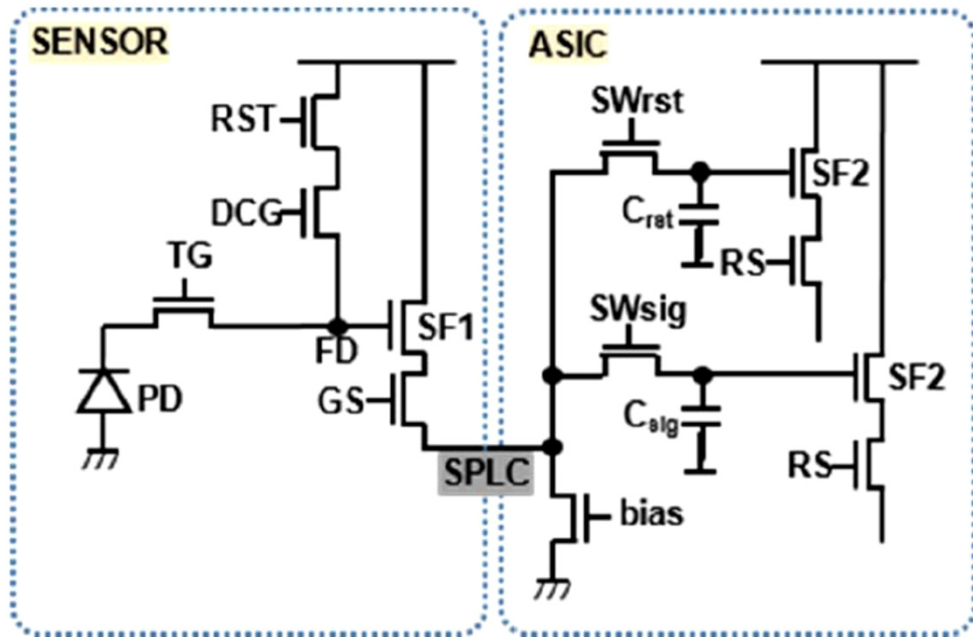


V. Venezia, IEDM 2018

Global Shutter Pixel with Stacked Circuitry

- Stacked pixel circuitry enables low-voltage domain GS pixel

-100 dB PLS @2.2- μm GS pixel
i.e., Shutter efficiency: 100dB

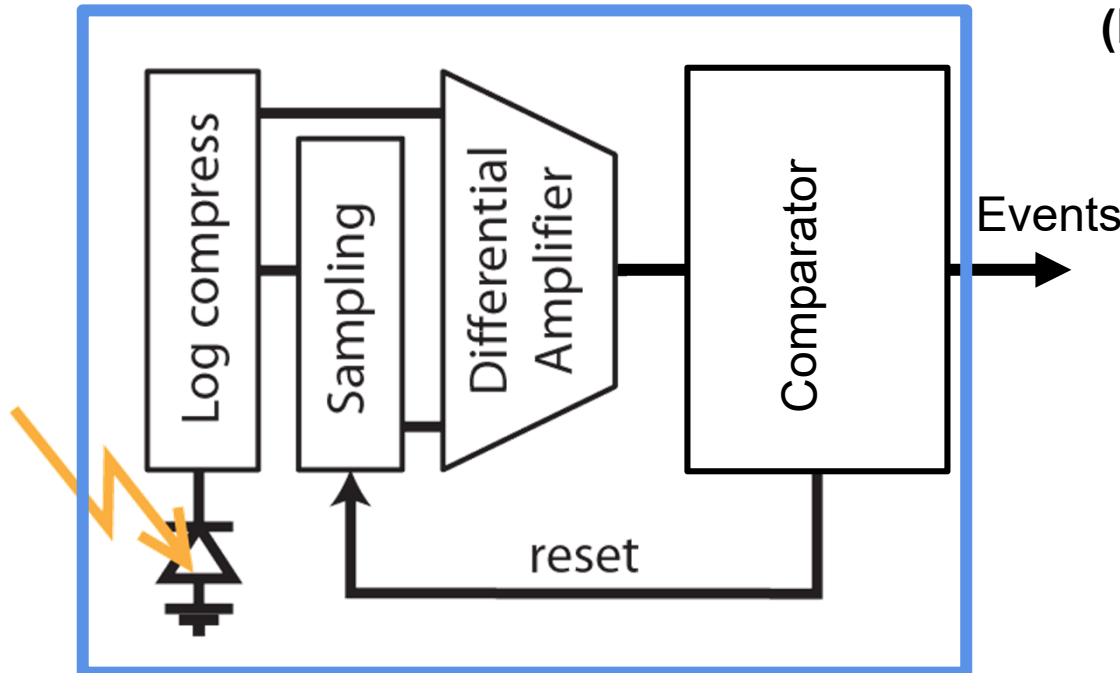


G. Park, IEDM 2019

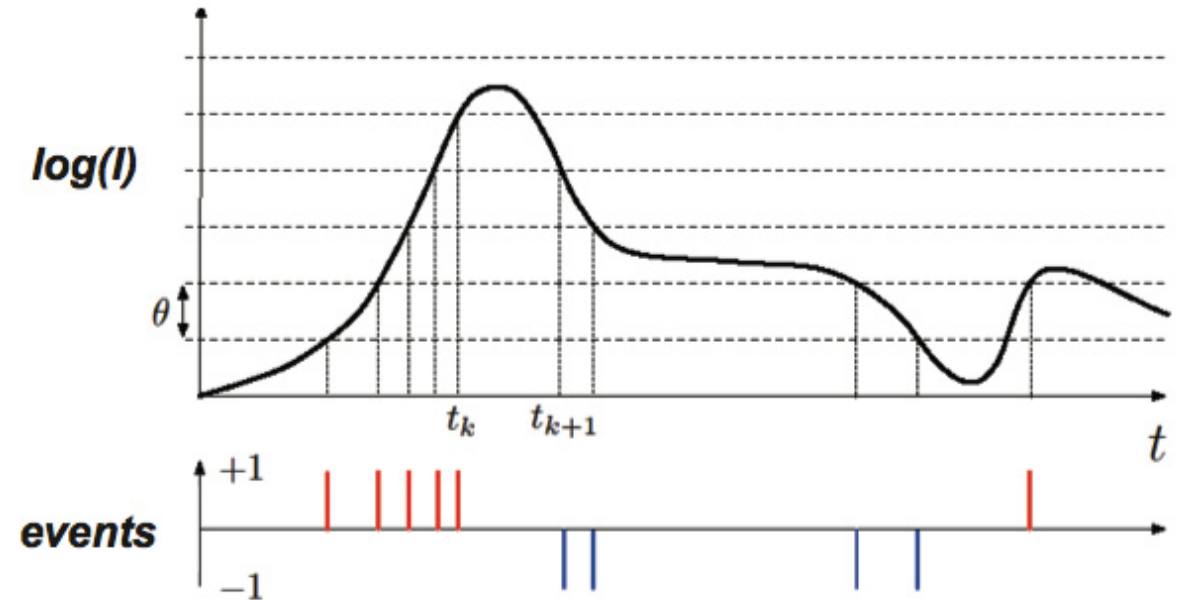
Event-based Vision Sensor (EVS)

- Contrast change detector implemented in pixel-level circuitry

Pixel



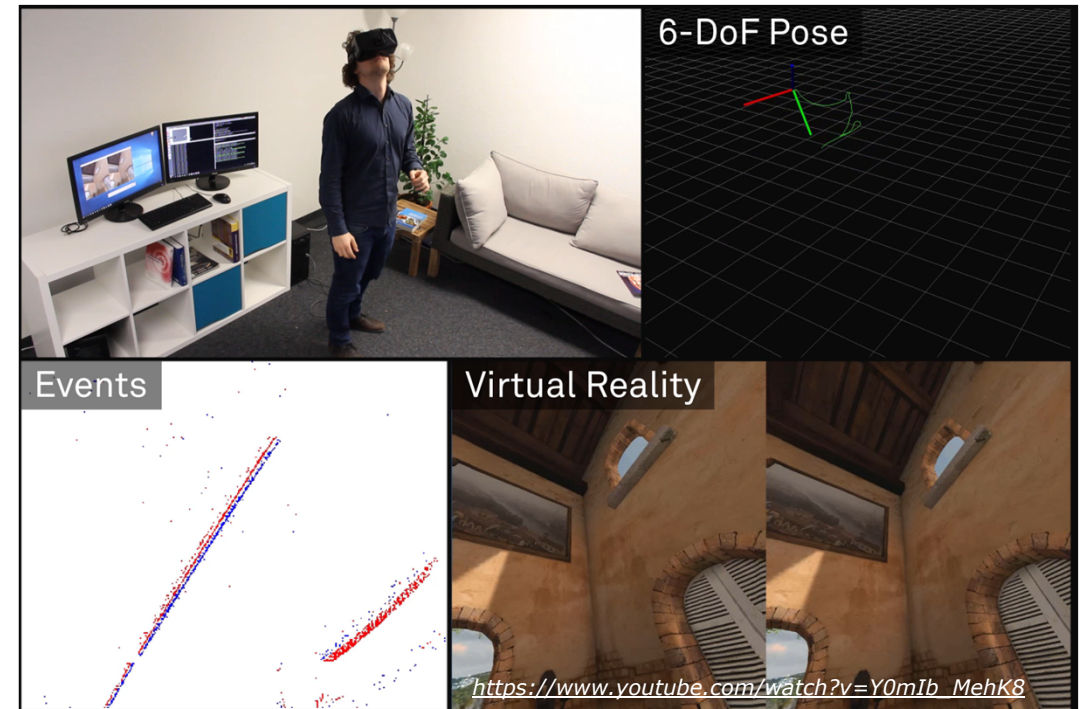
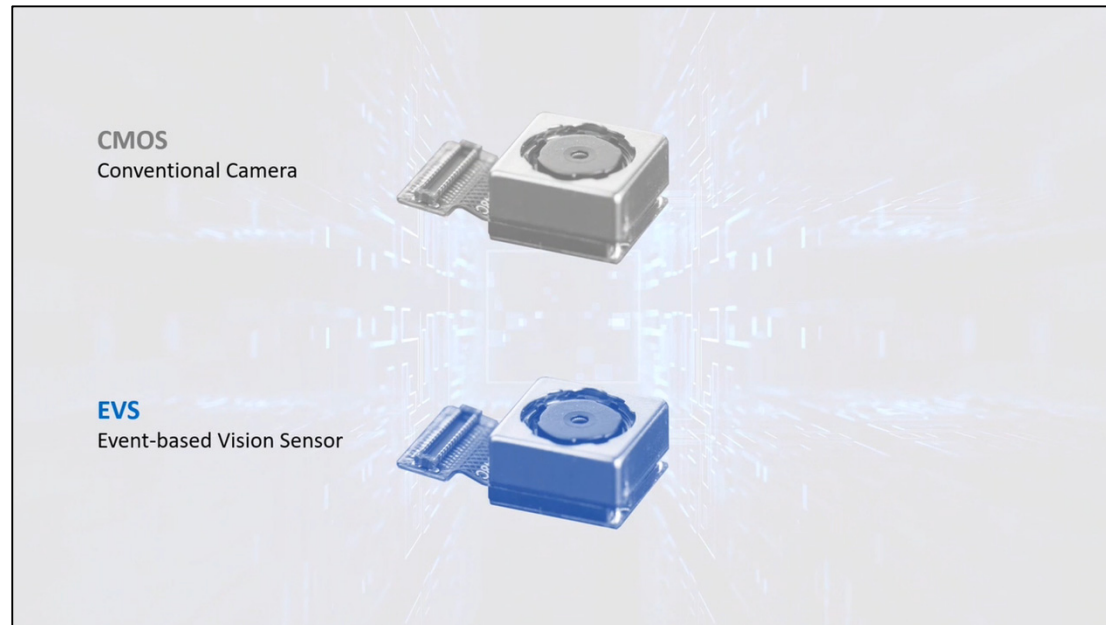
Photocurrent (Incident intensity)



Video

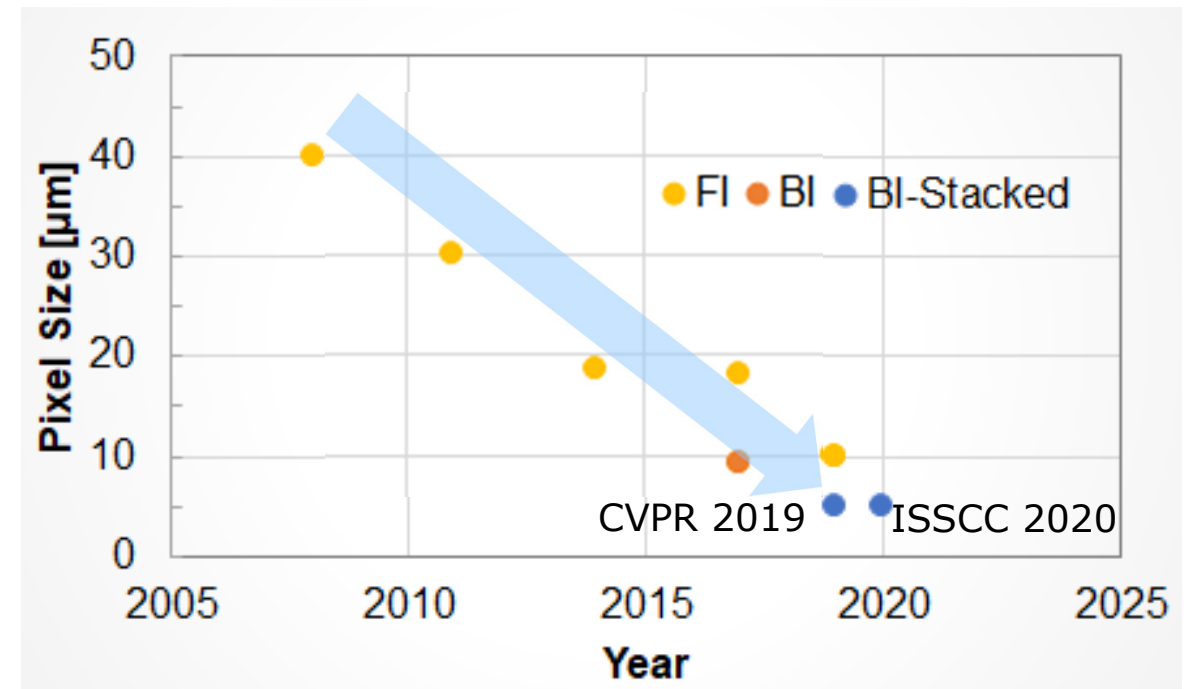
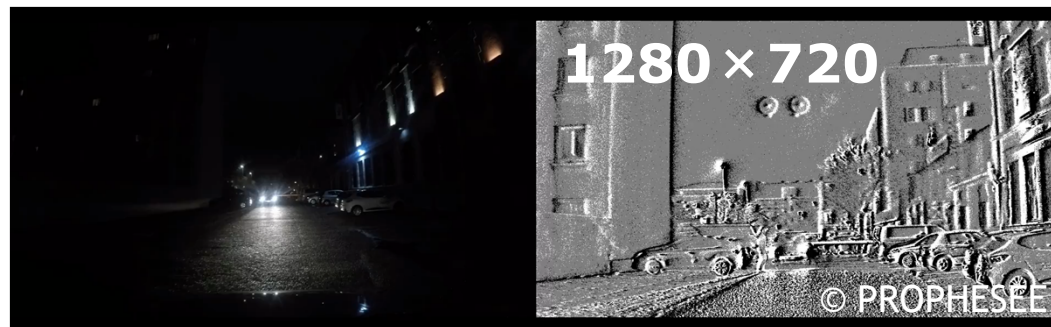
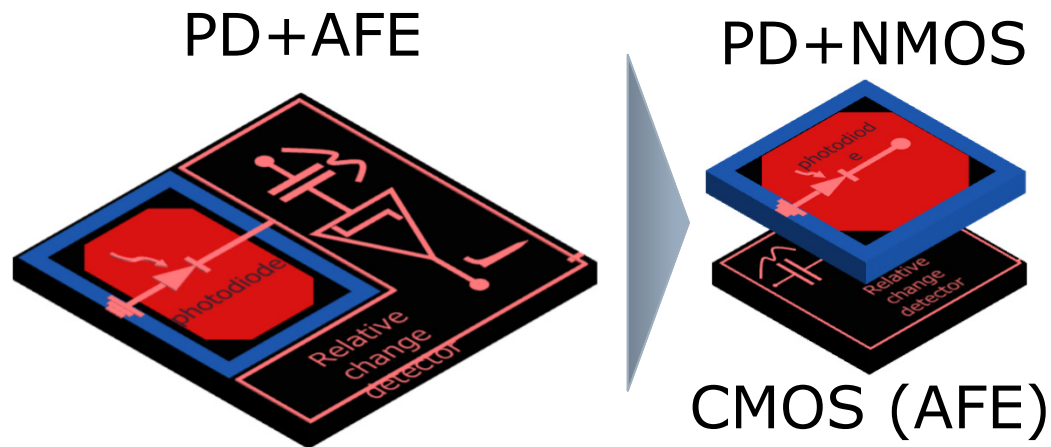
Event-based Vision Sensor (EVS)

- Offers compressed data with low latency and low power



Back-illuminated Stacked EVS

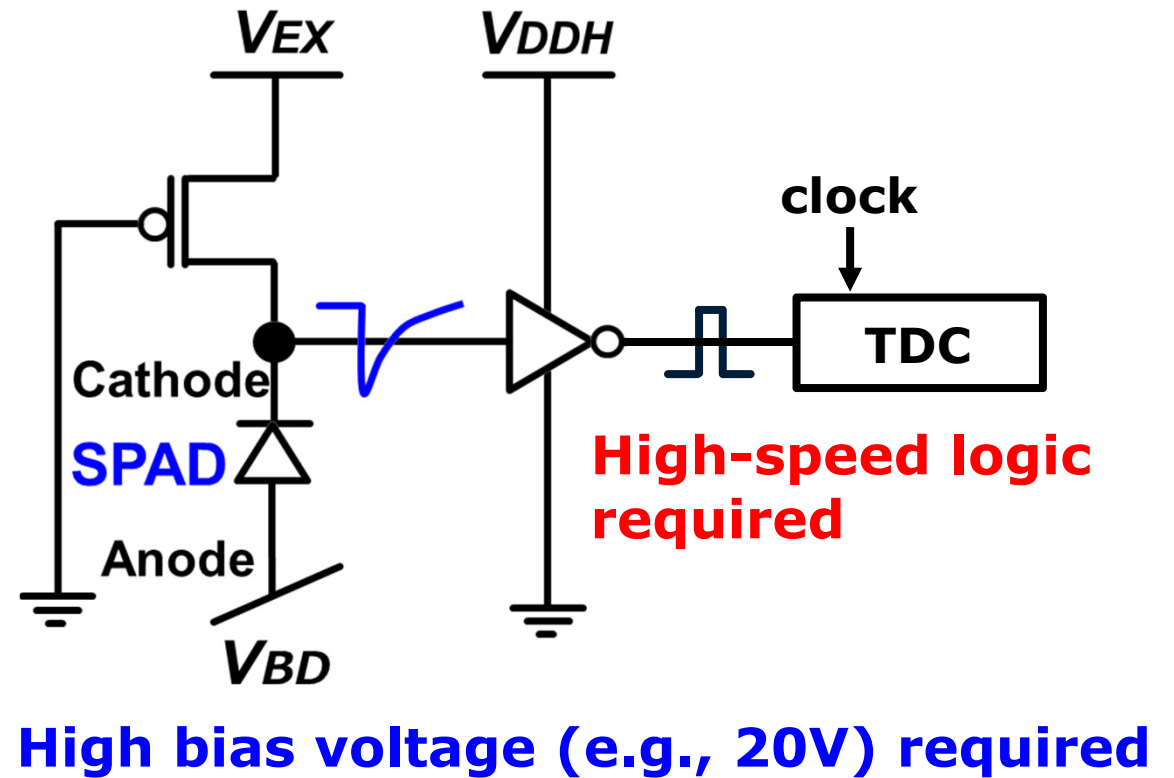
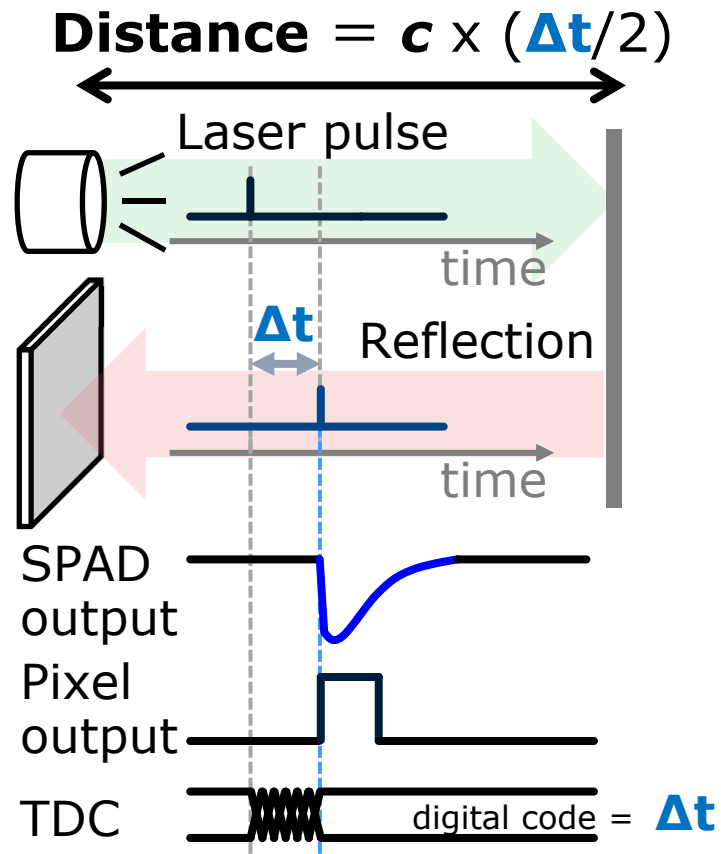
- Fine-pitch Cu-Cu connections enable implementation of pixel-parallel functionality to realize practical applications



T. Finateu, ISSCC 2020

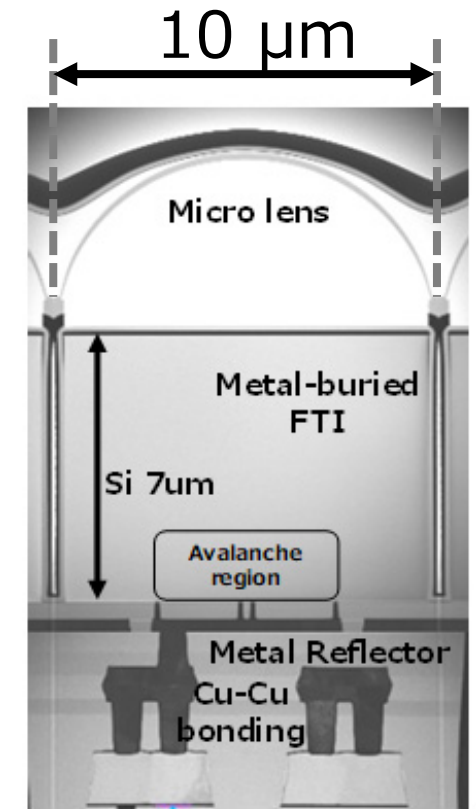
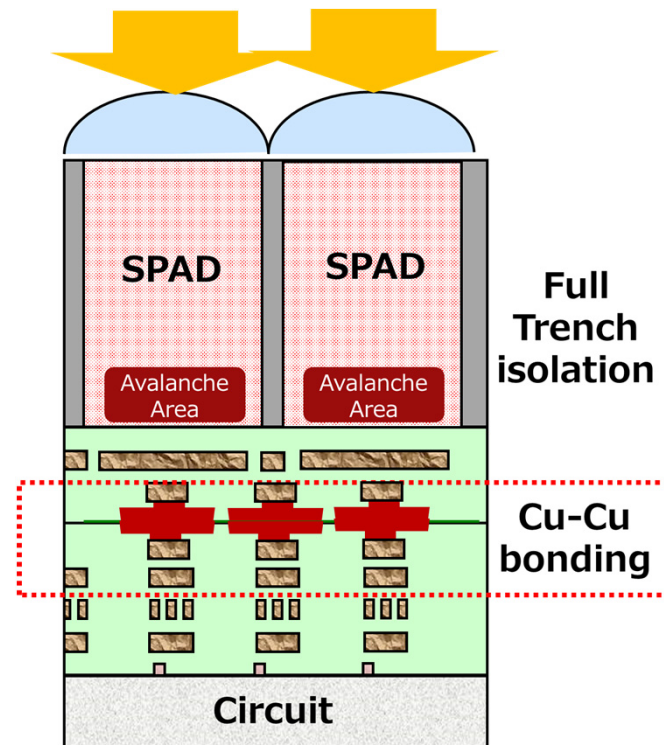
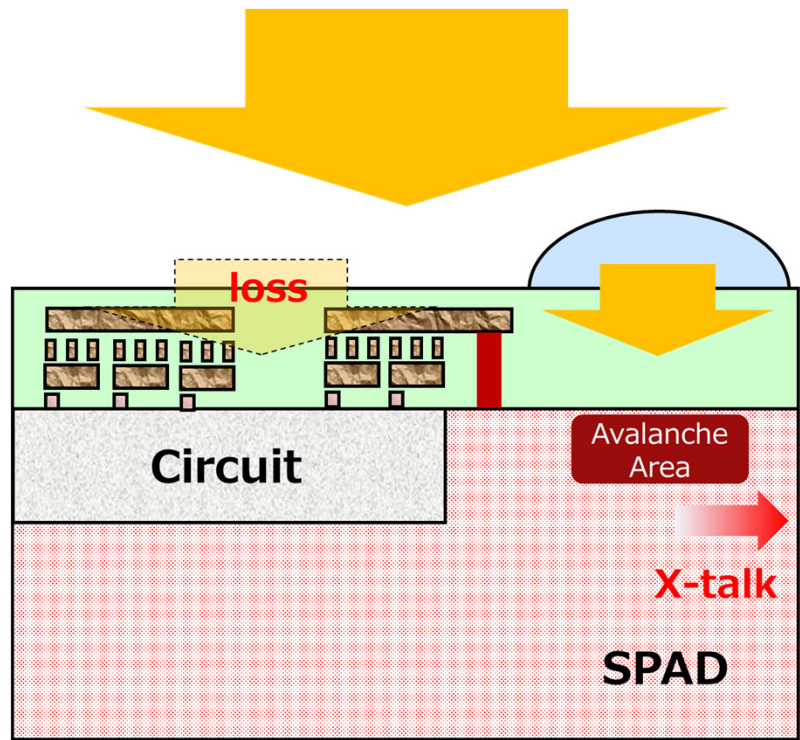
SPAD-based Direct ToF (dToF)

- Requires high bias voltage at SPAD and high-speed logic circuits



SPAD with Cu-Cu Bonding

- BI stack is promising breakthrough of SPAD technology to enter wider market fields

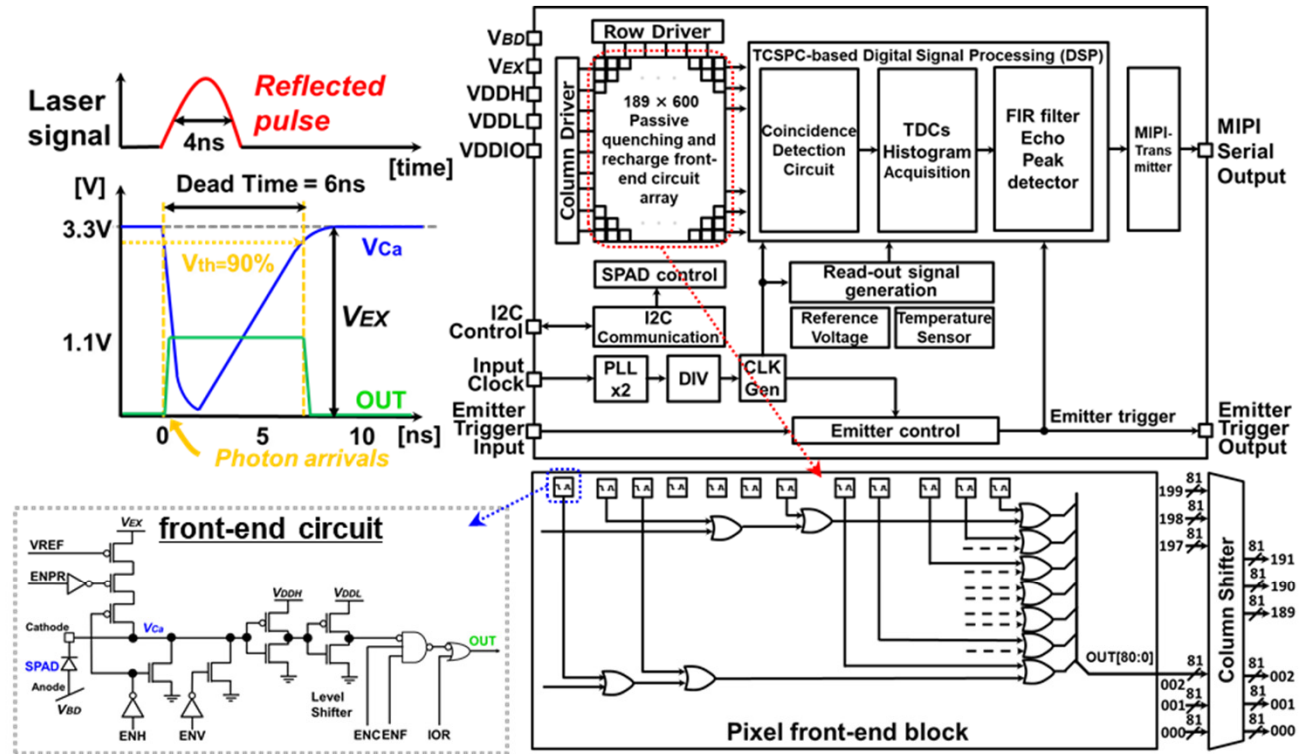
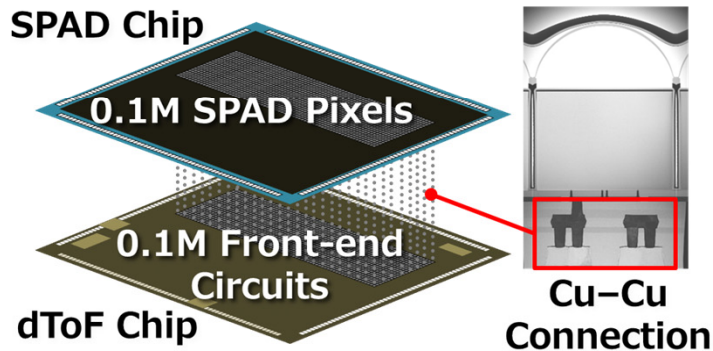
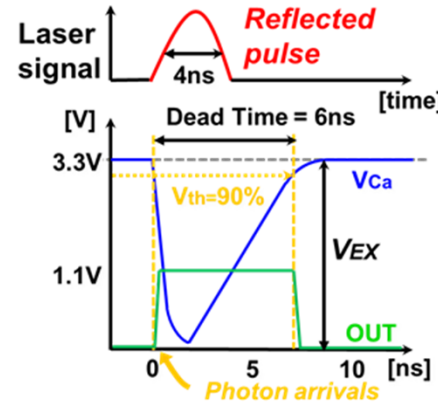
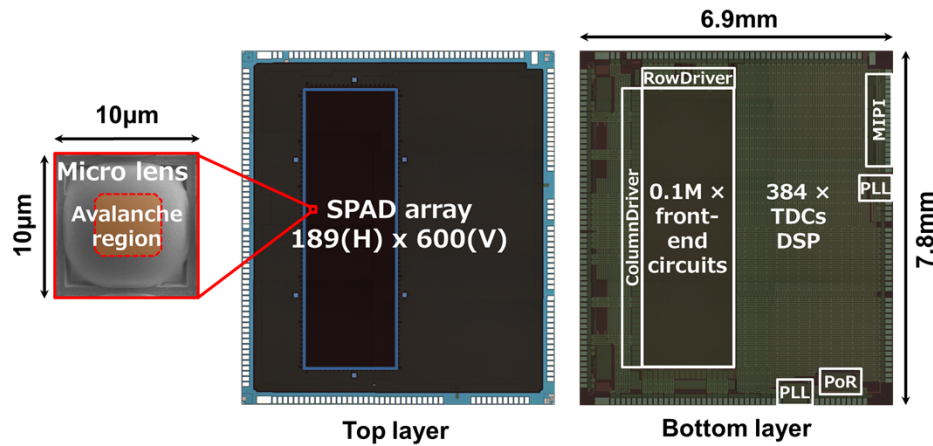


K. Ito, IEDM 2020

Back-illuminated Stacked dToF Sensor

- Optimized process technologies applicable to SPAD and logic

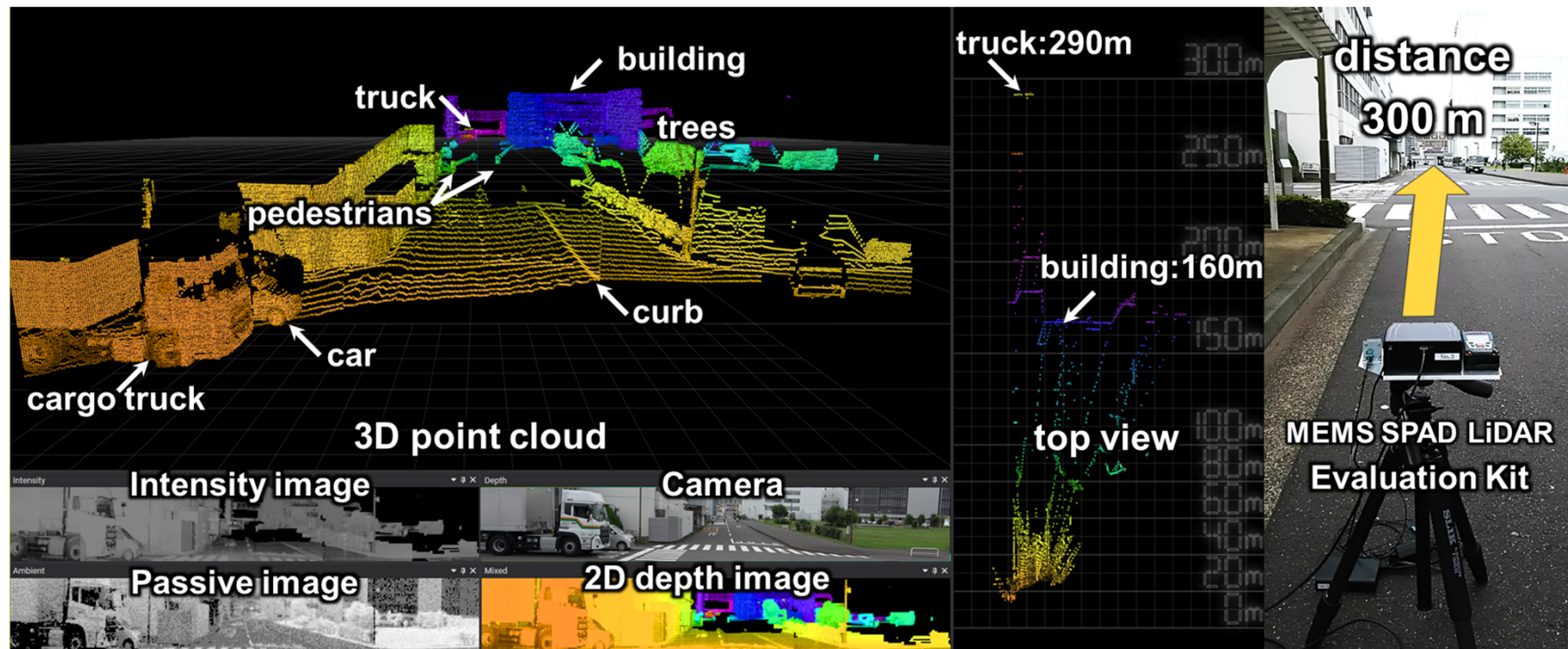
90nm SPAD 40nm logic



To be presented by O. Kumagai, ISSCC 2021

Back-illuminated Stacked dToF Sensor

- Highly integrated on-chip signal processor with optimized SPAD device process and TDCs yields superior LiDAR solution



To be presented by O. Kumagai, ISSCC 2021

Possibilities of Architectural Change

- Pixel parallel architecture is becoming reality.

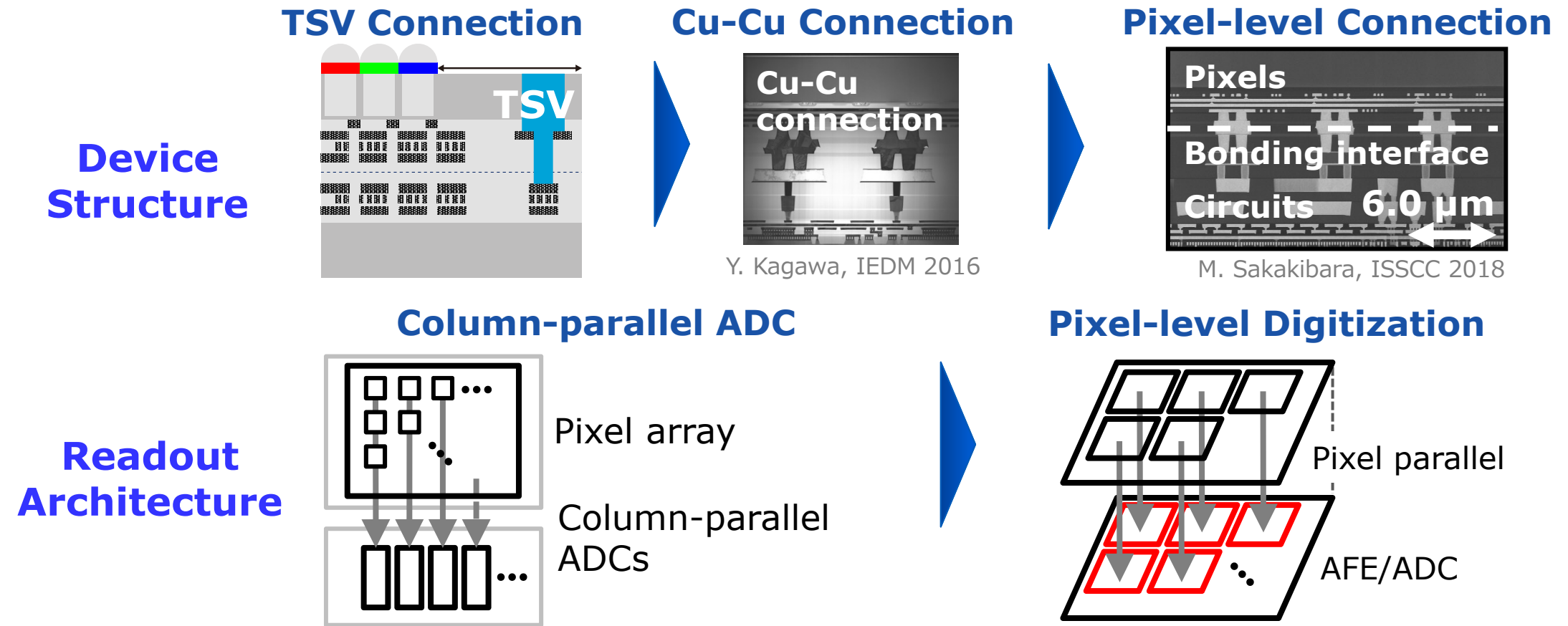
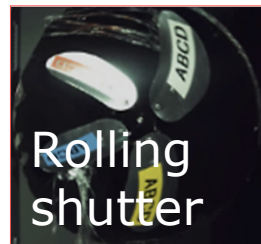
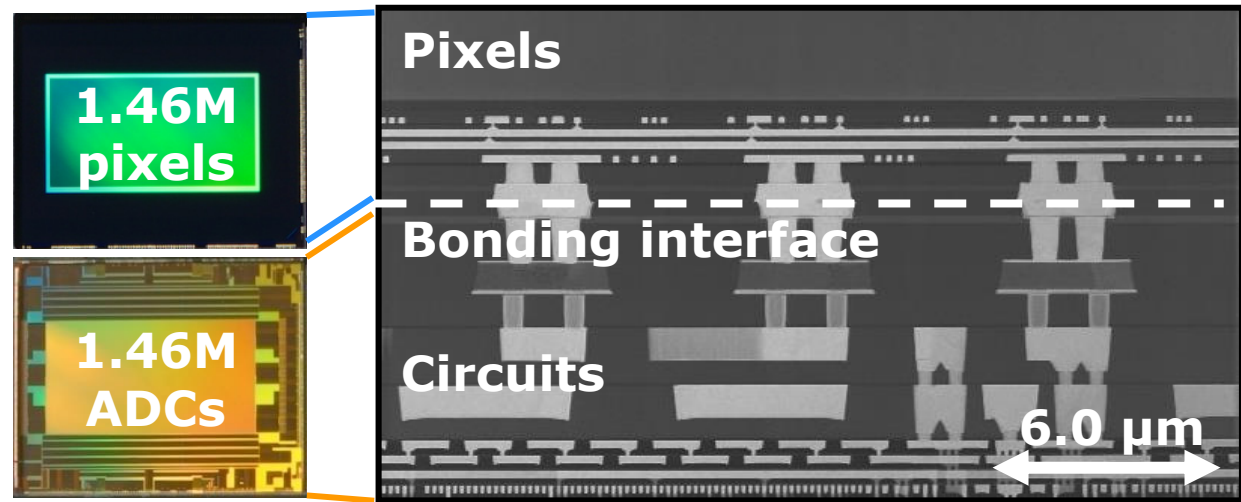
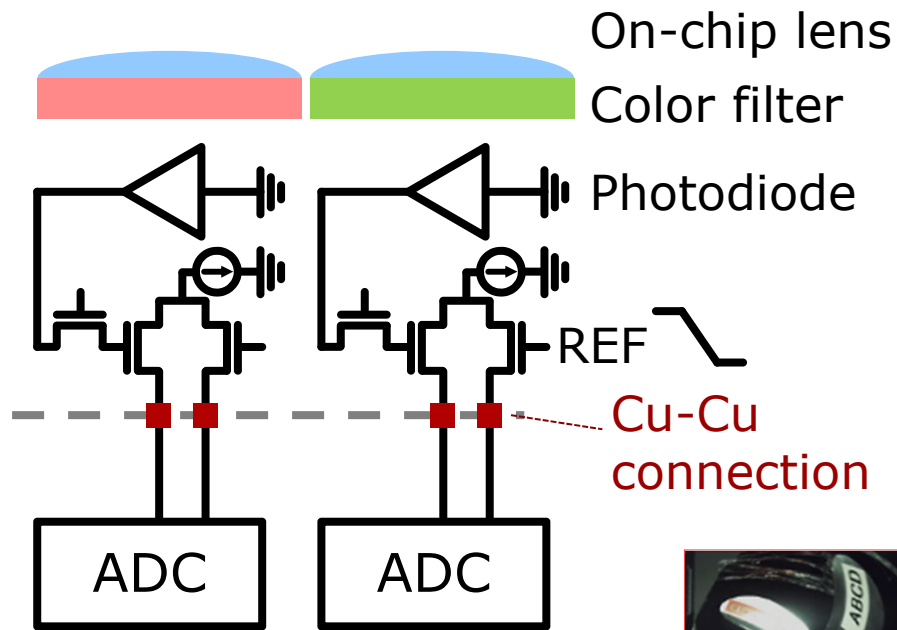


Image Sensor with Pixel-parallel ADC

- Over 1 million ADCs have been mounted in pixel-parallel arrangement

2 interconnections in 6.9- μm pitch pixel.

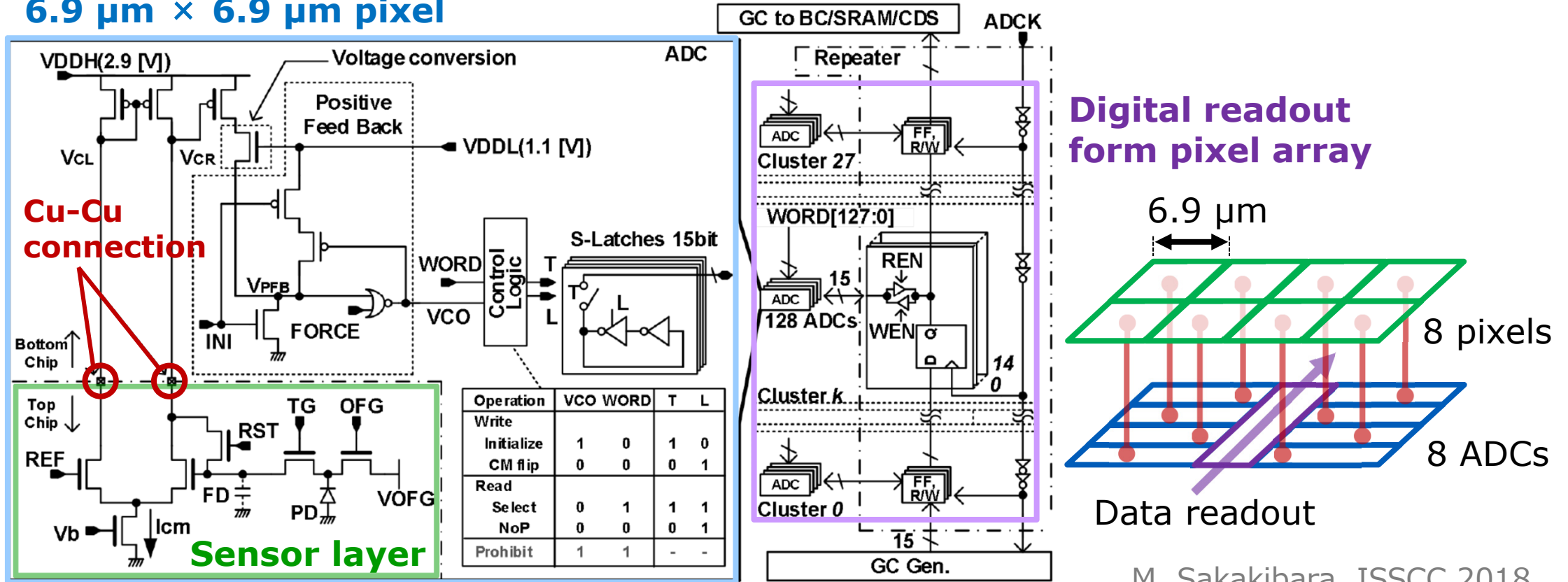


M. Sakakibara, ISSCC 2018

Pixel-parallel ADC Implementation

- Single-slope ADC is directly connected to pixel amp transistors

6.9 μm \times 6.9 μm pixel

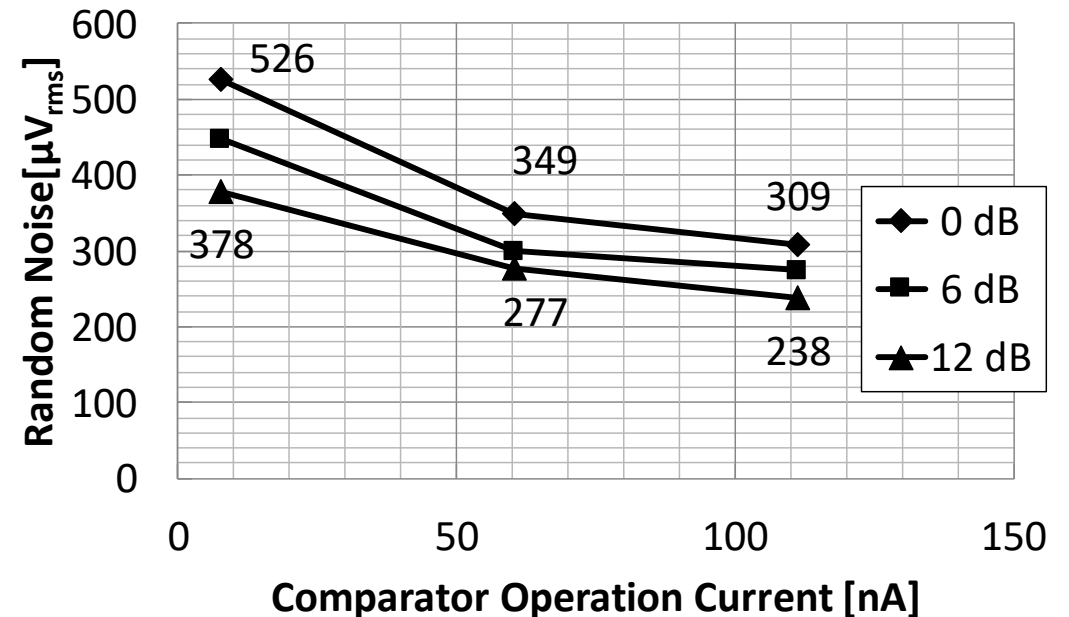
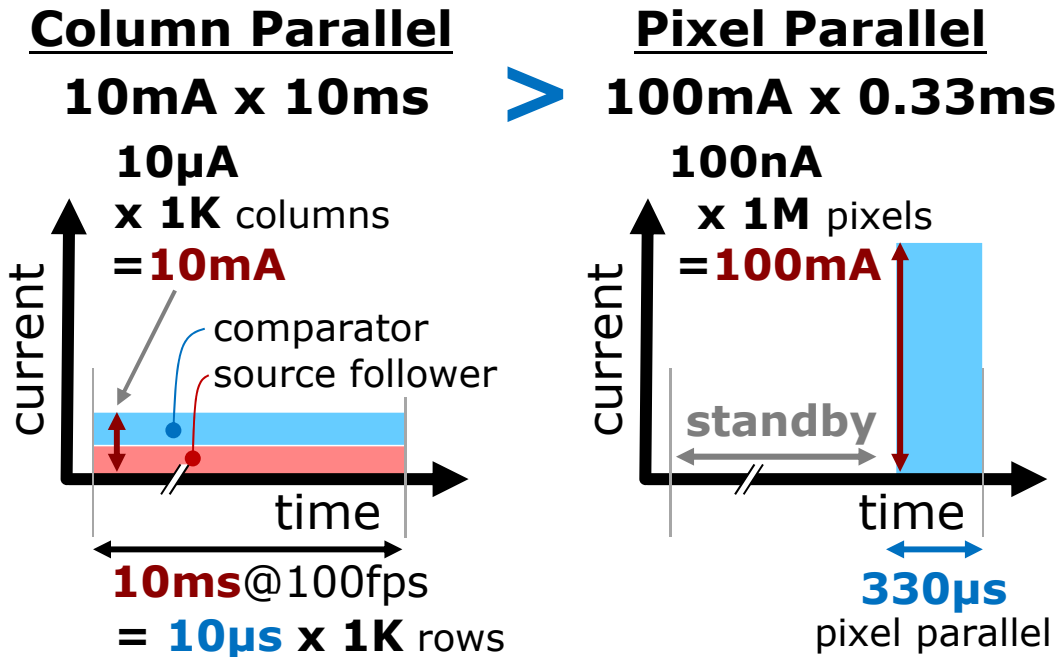


M. Sakakibara, ISSCC 2018

Pixel-parallel ADC Features

- Allows band limitation with $\sim 300 \mu\text{V}_{\text{rms}}$ readout noise at 100-nA-comparator operation for high-speed global-shutter imaging

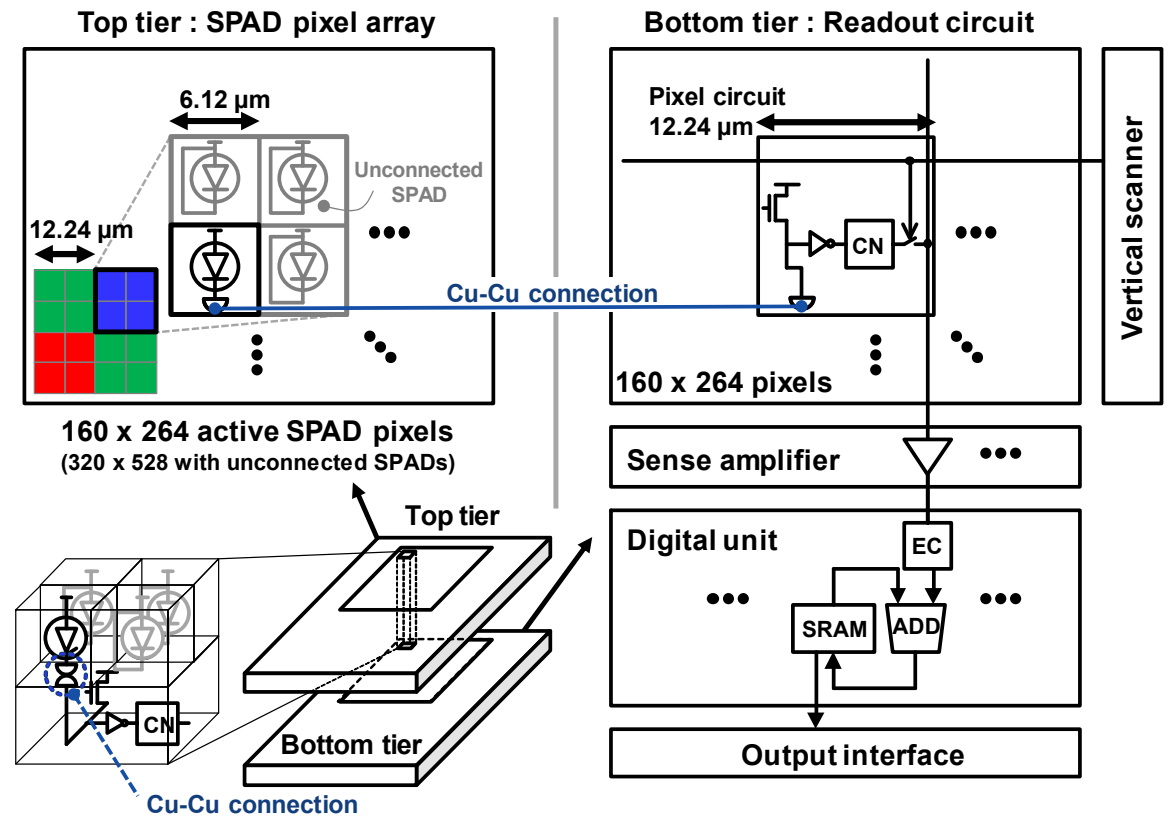
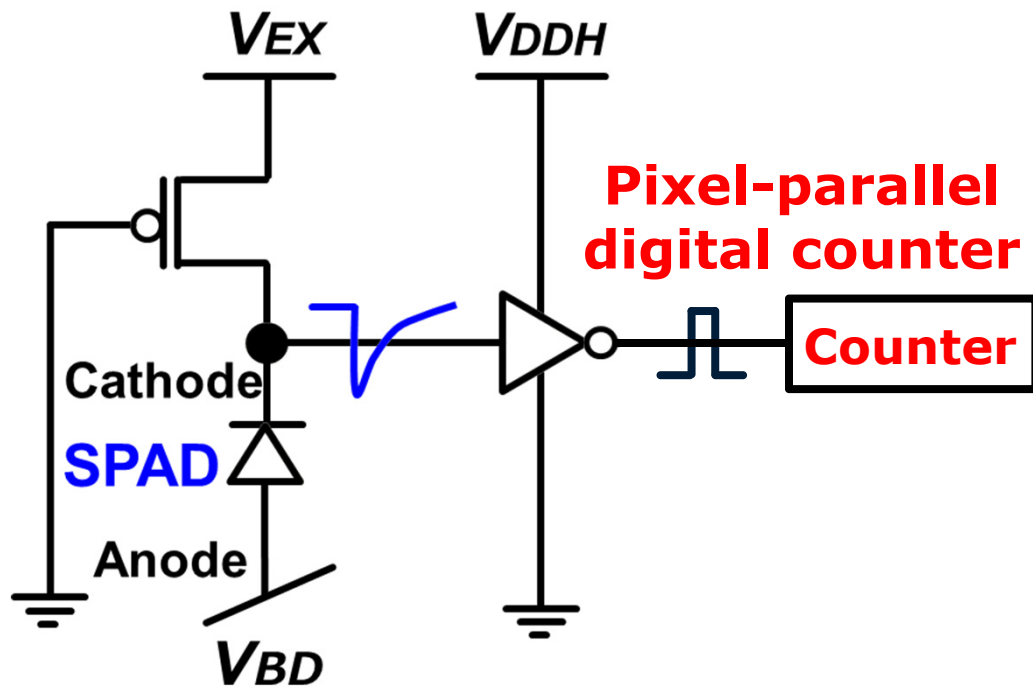
Rough estimation of power consumption at 100 fps



M. Sakakibara, ISSCC 2018

Photon Counting Image Sensor

- 3D integration provides possibility of practical photon count imaging

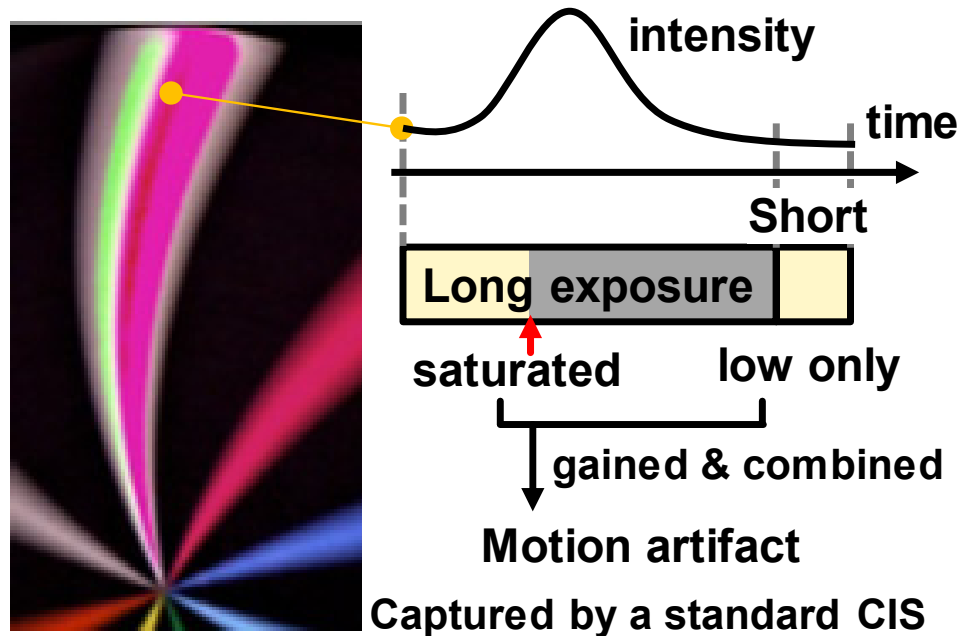


To be presented by J. Ogi, ISSCC 2021

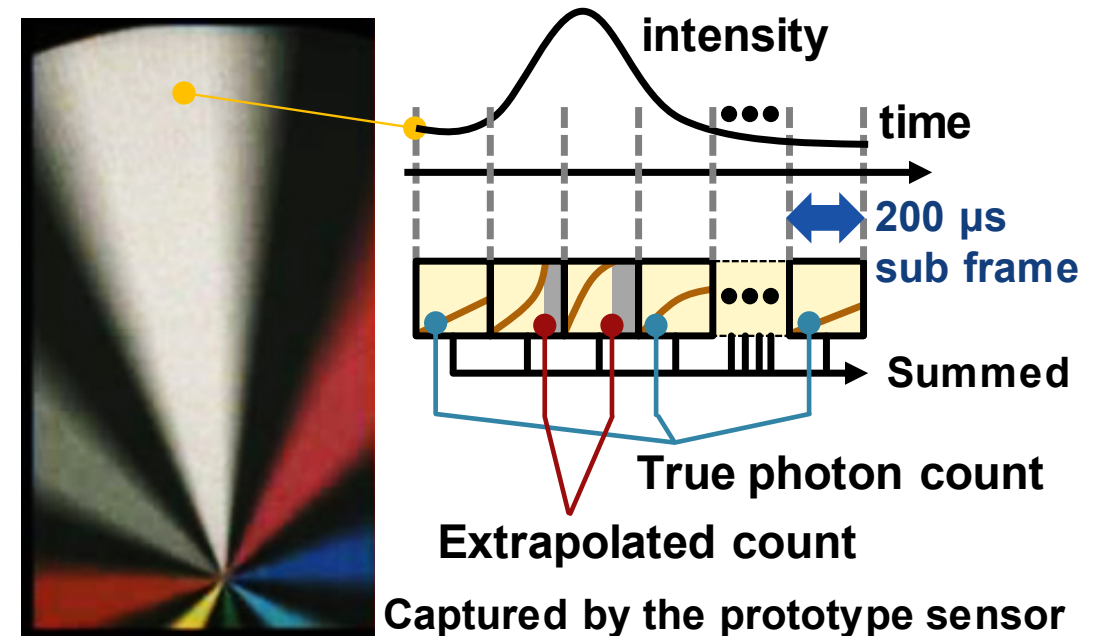
Photon Counting Image Sensor

- Pixel-parallel instant digitization can extend functionality

Conventional multiple exposure



Sub-frame extrapolating architecture

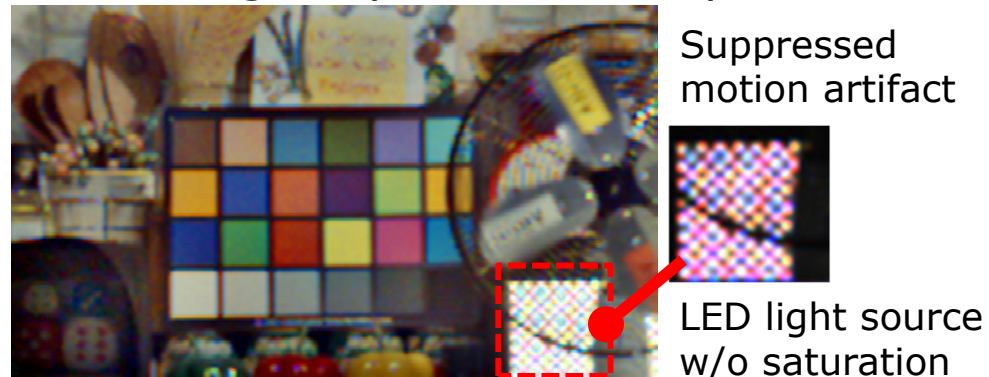


To be presented by J. Ogi, ISSCC 2021

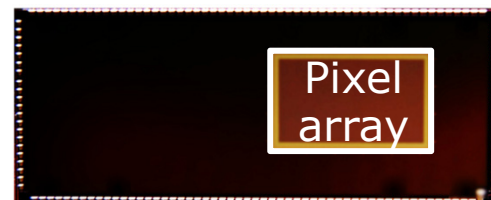
Photon Counting Image Sensor

- Pixel-parallel instant digitization has potential of GS and HDR

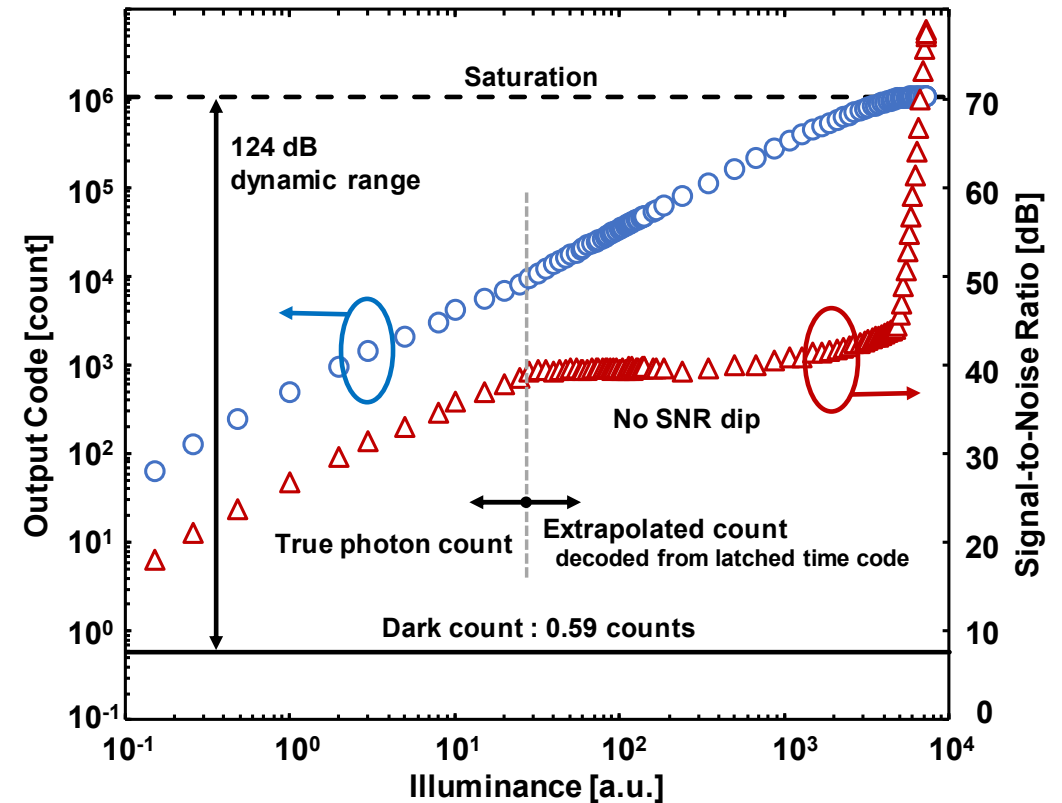
HDR image capture at 250 fps



Sensor chip



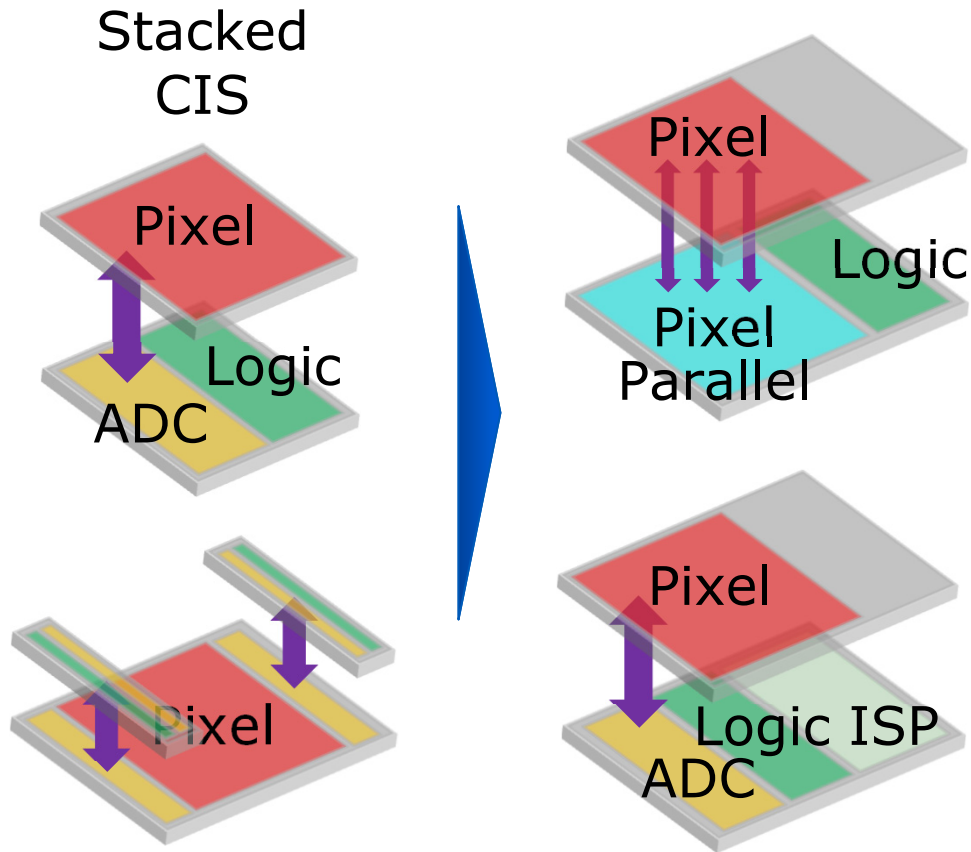
Logic chip



To be presented by J. Ogi, ISSCC 2021

Hybrid Integration on Si

- Sensor architecture is evolving using 3D technologies



More advanced pixel circuitry

- Stacked pixel circuitry
- Event-based vision sensing
- Pixel-parallel ADC architecture
- SPAD-based photon counting

Hybrid Integration on Si

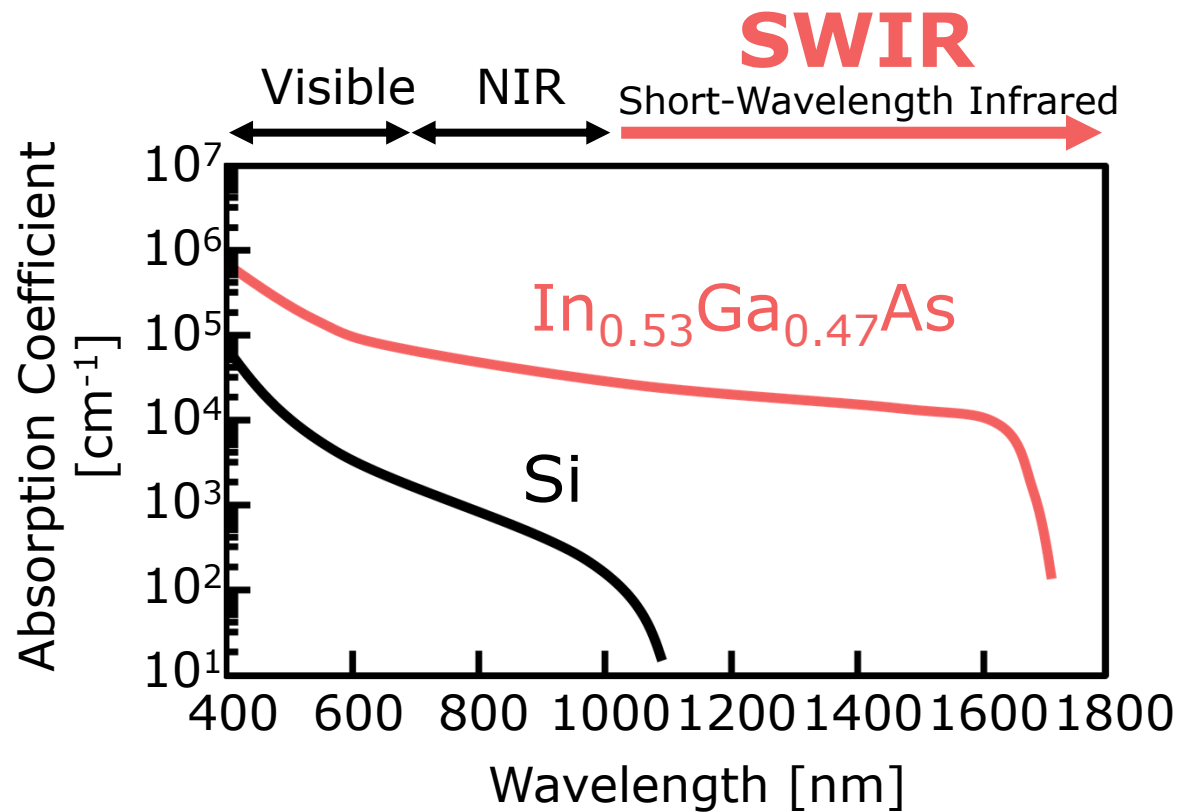
- SWIR InGaAs photodetector

Integrating more intelligent processor with sensor

- Intelligent vision sensor

Compound Semiconductor Photodetector

- Promising for future automated inspection and secured society



Si Imager

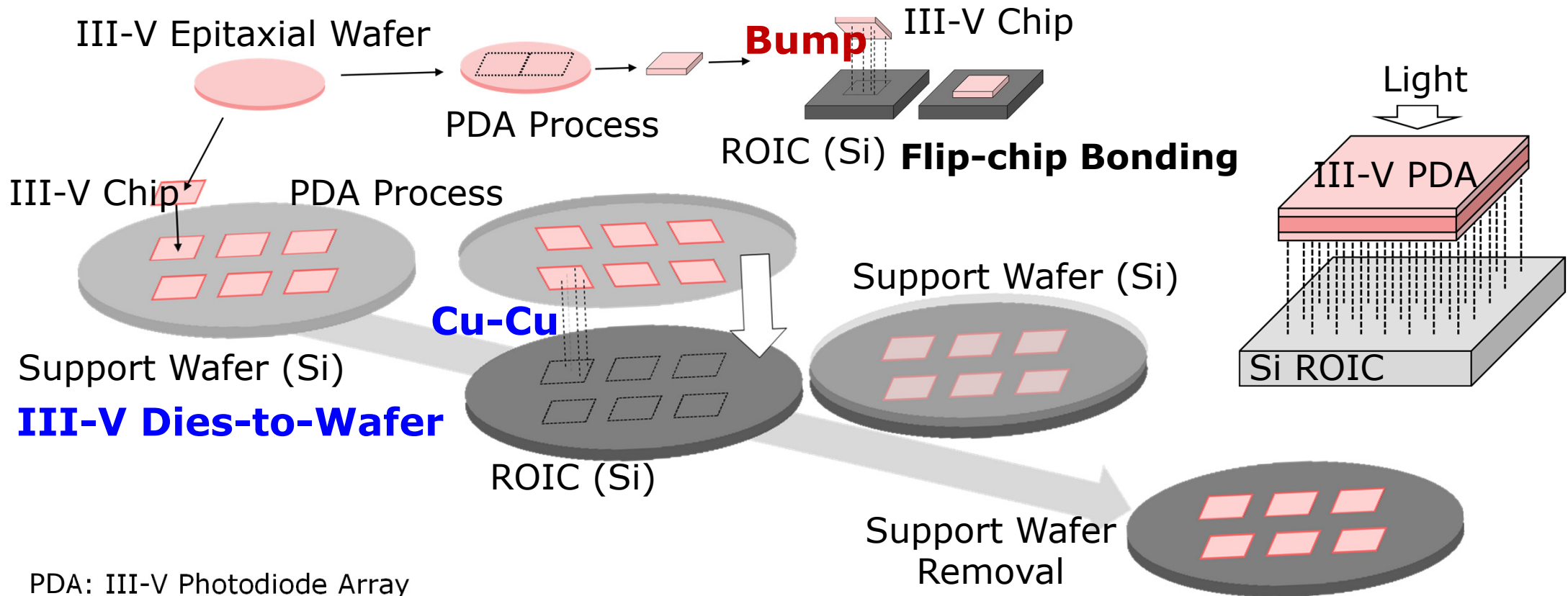


InGaAs Sensor



Hybrid III/V on Si Integration

- Compound semiconductor photodetector bonded on Si ROIC

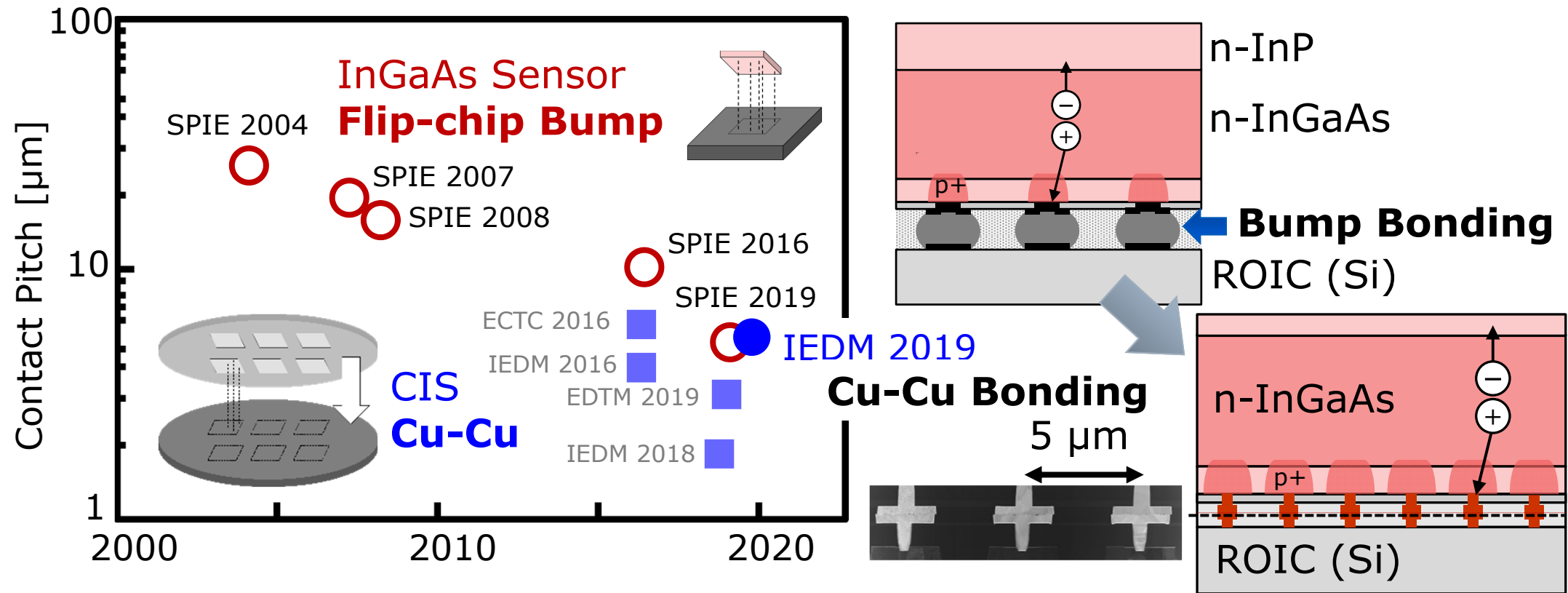


PDA: III-V Photodiode Array
ROIC: Read-out Integrated Circuit

S. Manda, IEDM 2019

Trend of Contact Pitch for III-V Photodetector

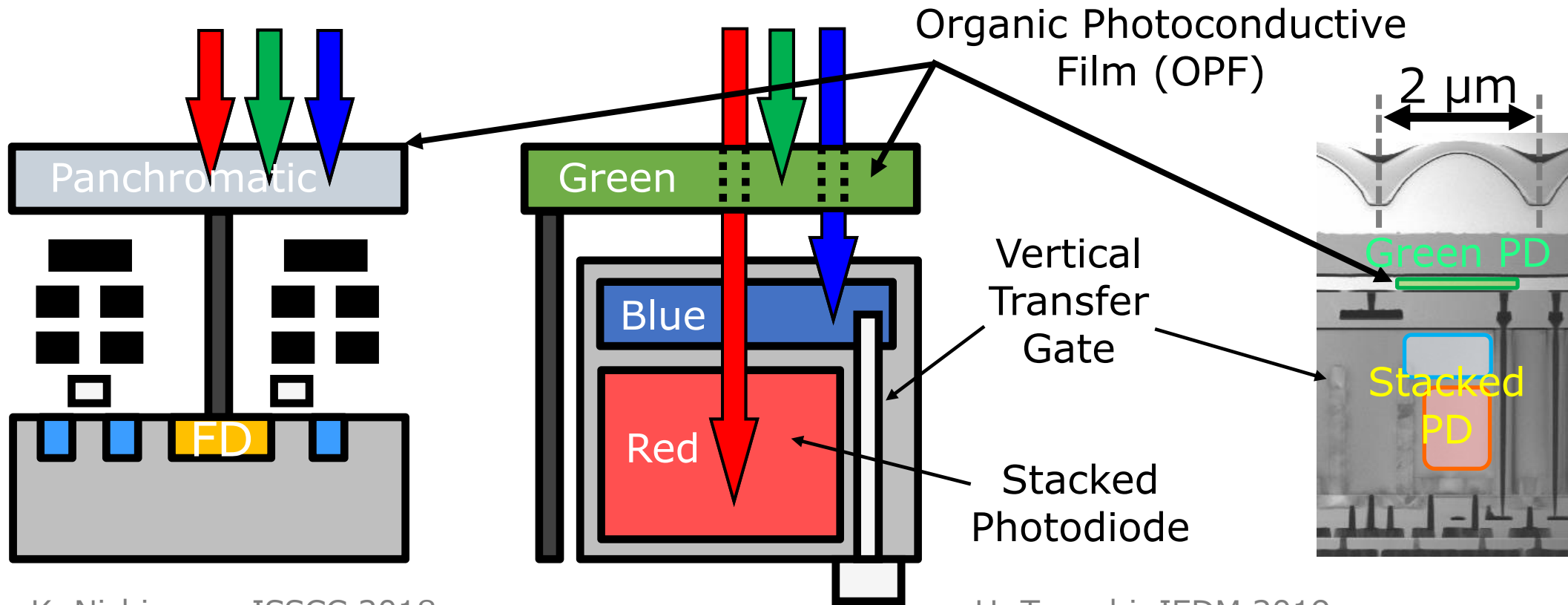
- Advanced bonding process evolving III-V detector integration



S. Manda, IEDM 2019

Organic Photoconductive Film Stacked on Si

- OPF stacked on Si provides more freedom to use of Si layer

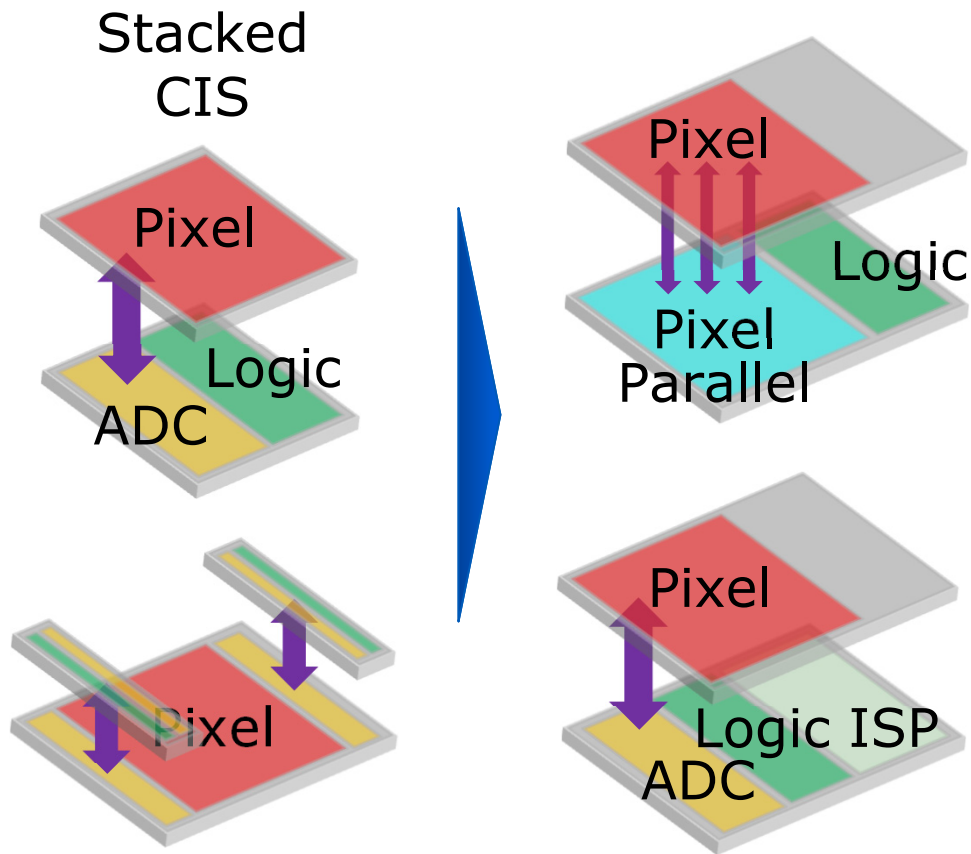


K. Nishimura, ISSCC 2018

H. Togashi, IEDM 2019

Integrating More Intelligent Processor with Sensor

- Sensor architecture is evolving using 3D technologies



More advanced pixel circuitry

- Stacked pixel circuitry
- Event-based vision sensing
- Pixel-parallel ADC architecture
- SPAD-based photon counting

Hybrid Integration on Si

- SWIR InGaAs photodetector

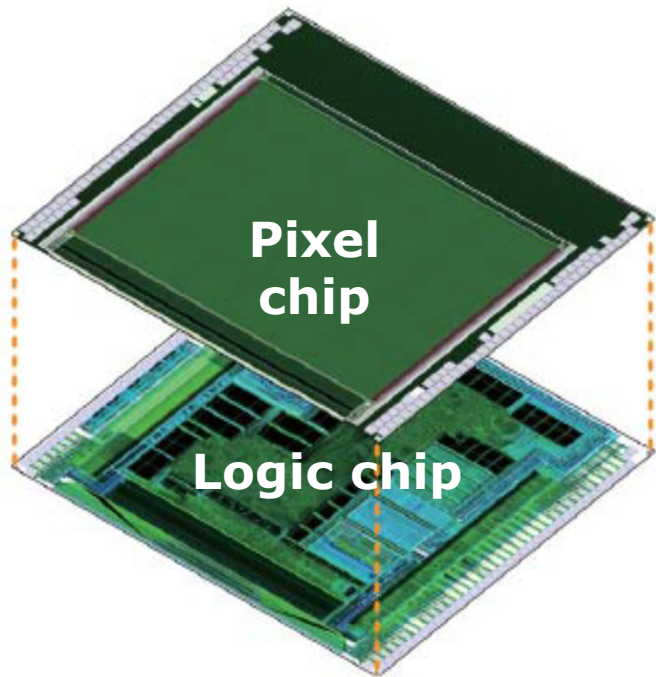
Integrating more intelligent processor with sensor

- Intelligent vision sensor

Integrated Edge AI

- Application of image sensors expanding by AI

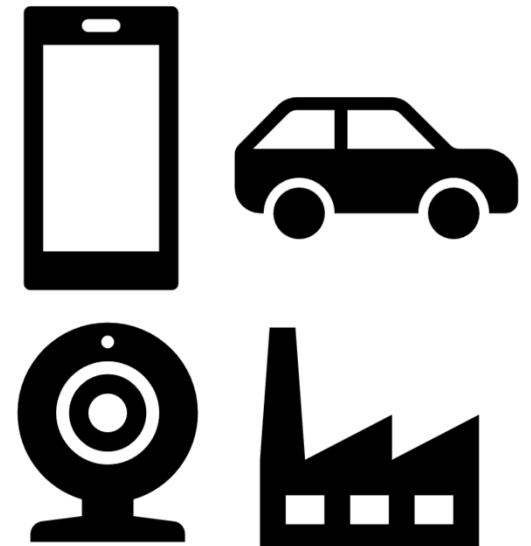
Image Sensor



AI



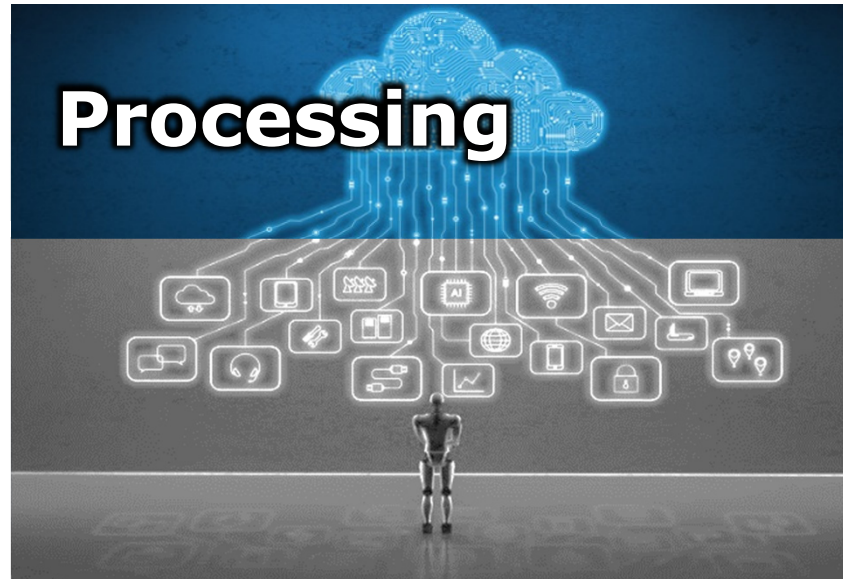
Applications



Integrated Edge AI

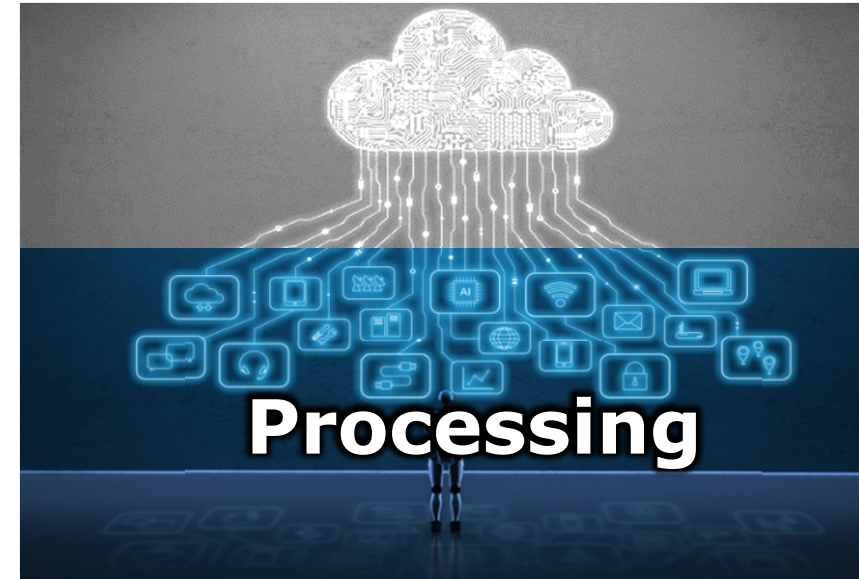
- Opportunities of edge AI integration with image sensor

Cloud AI



- Big data capability
- Unified performance

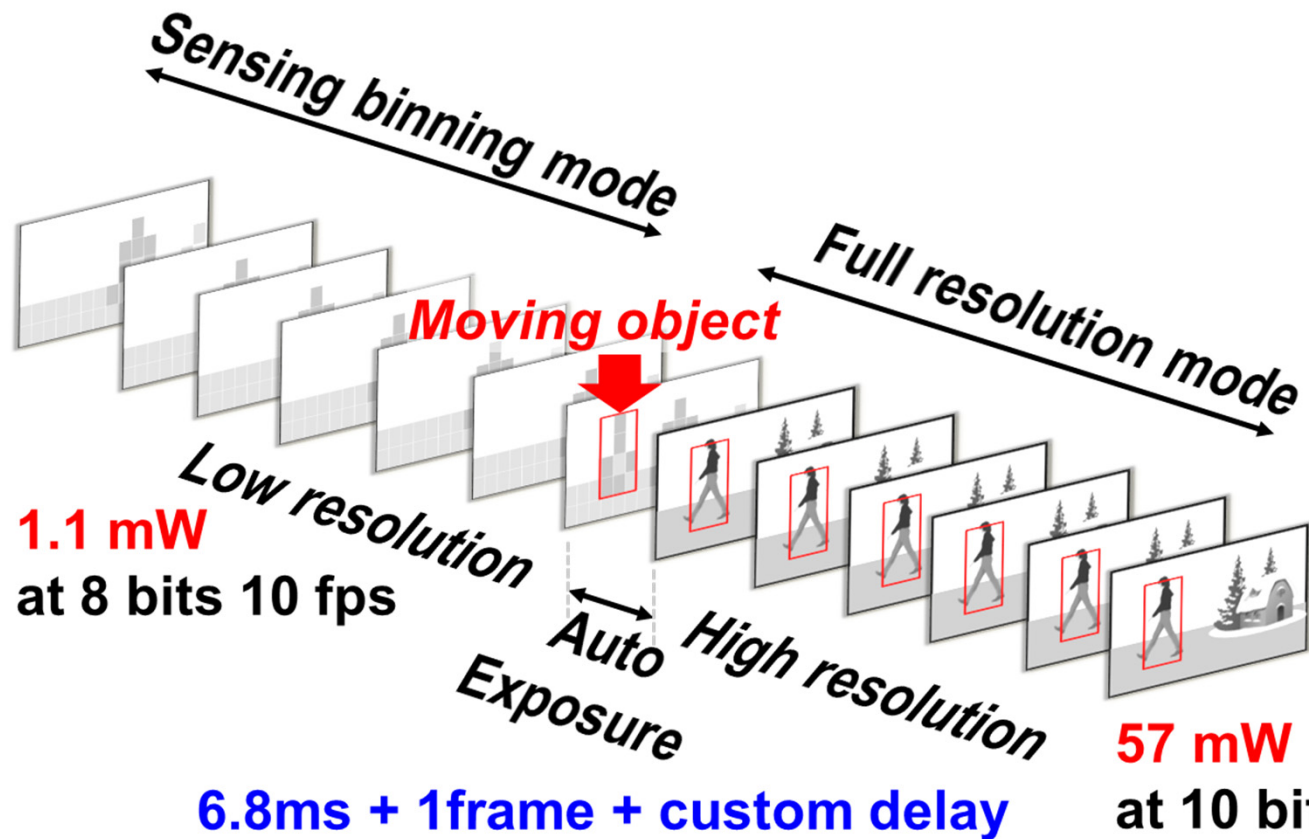
Edge AI



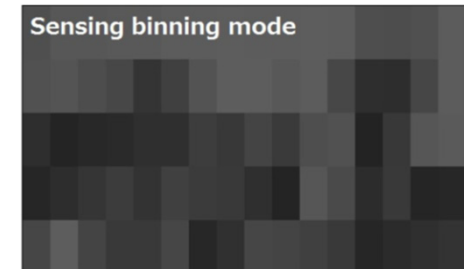
- Low latency/low bandwidth
- Privacy
- Low cloud cost

Always-on Monitoring Sensor

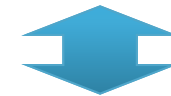
- Low-power always-on monitoring required at edge camera



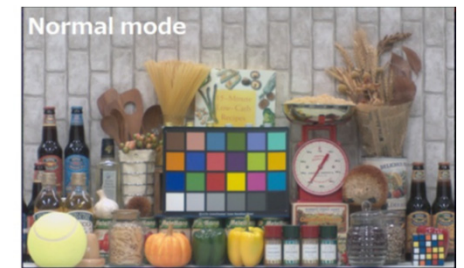
1.1 mW



Sensing mode 16x5 pixel



57 mW

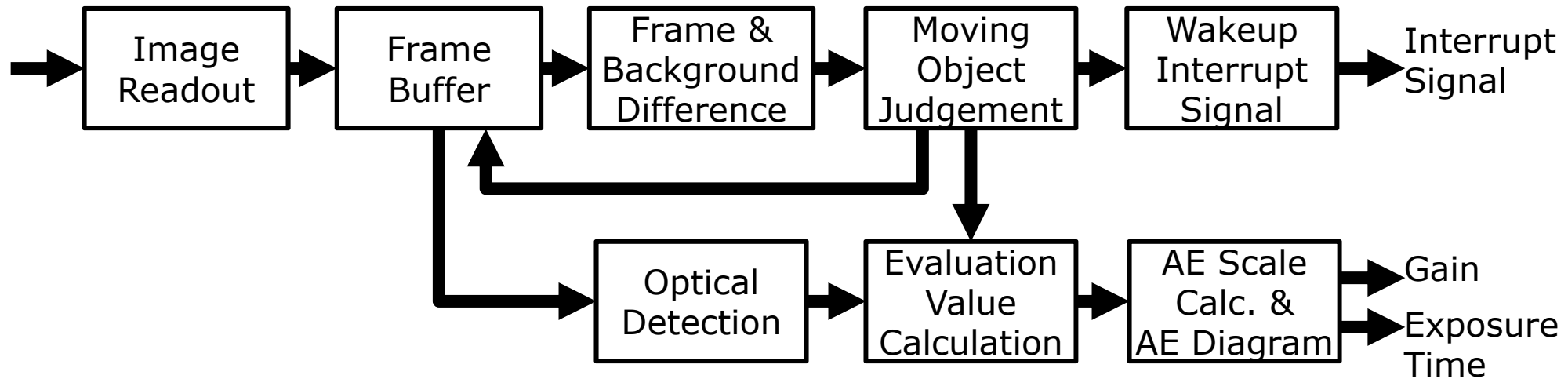


All pixel imaging 3.9M pixel

O. Kumagai, ISSCC 2018

Moving Object Detection Flow

- Moving object detection and wakeup process conducted on sensor



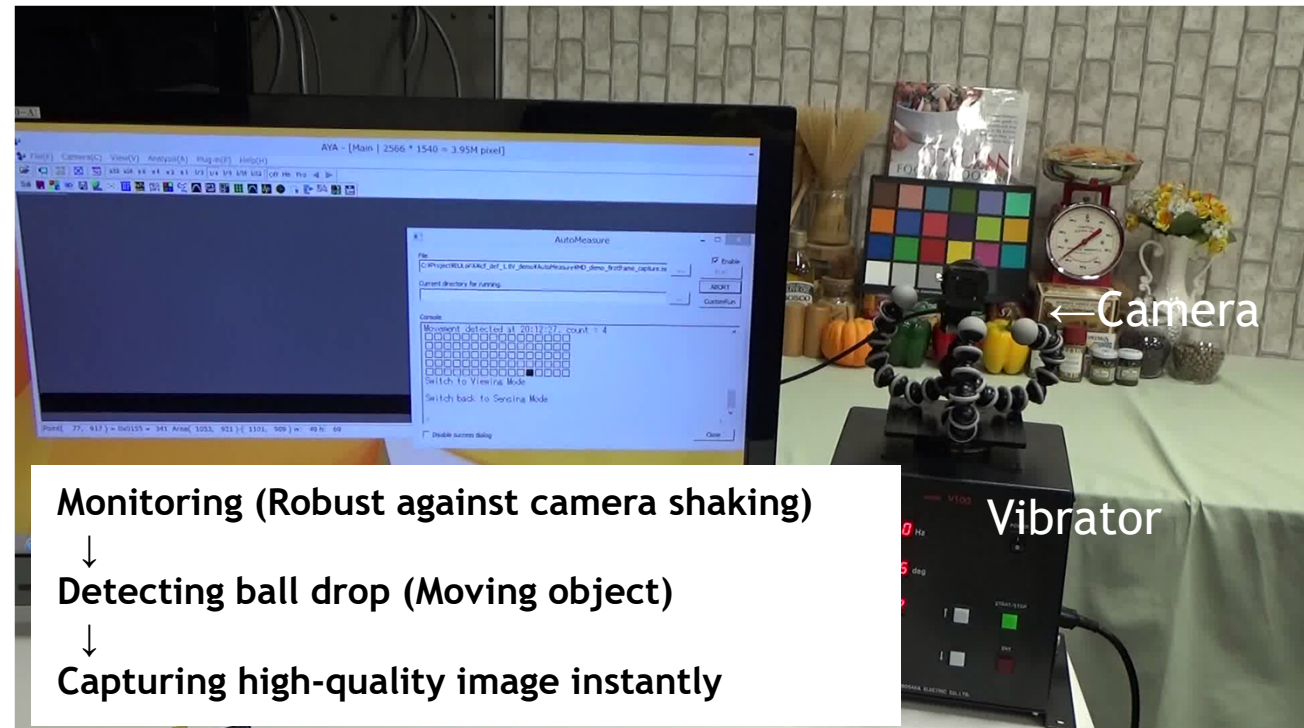
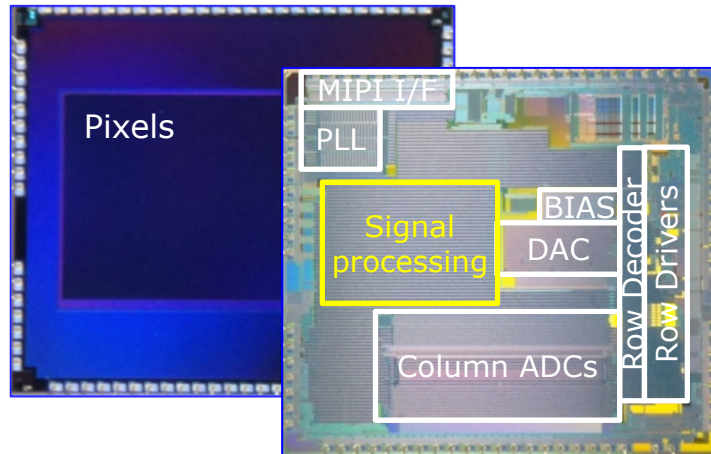
O. Kumagai, ISSCC 2018

Demonstration of Always-on Monitoring

- Low power always-on detection integrated in stacked sensor



Passenger detection experiment = 100%

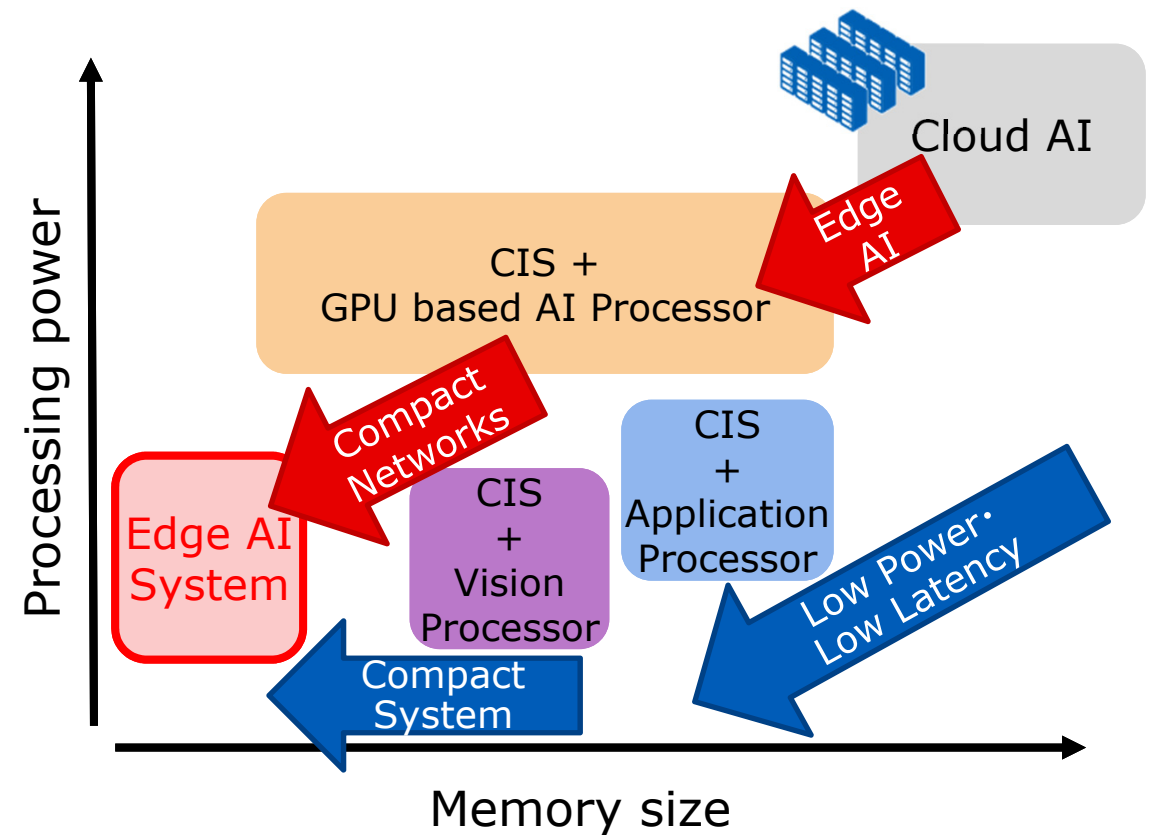
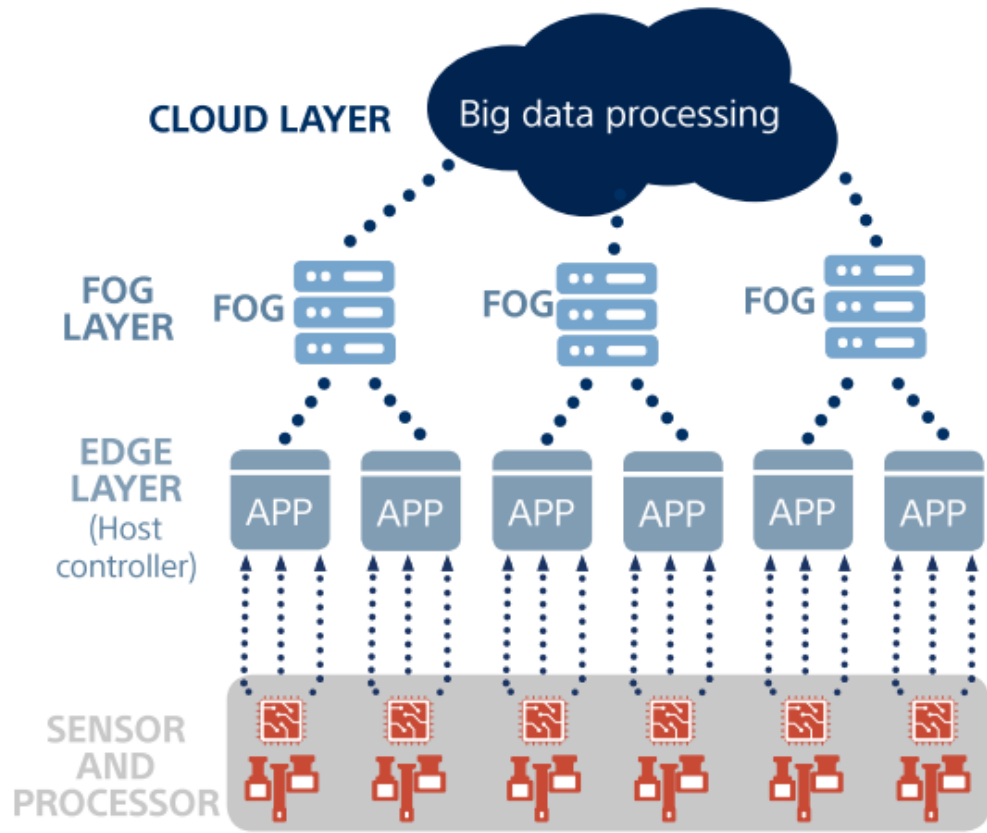


Video

O. Kumagai, ISSCC 2018

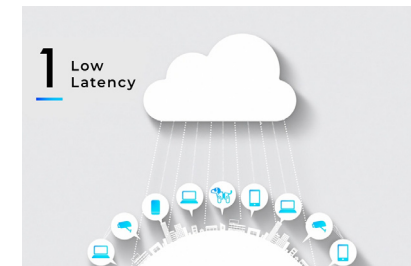
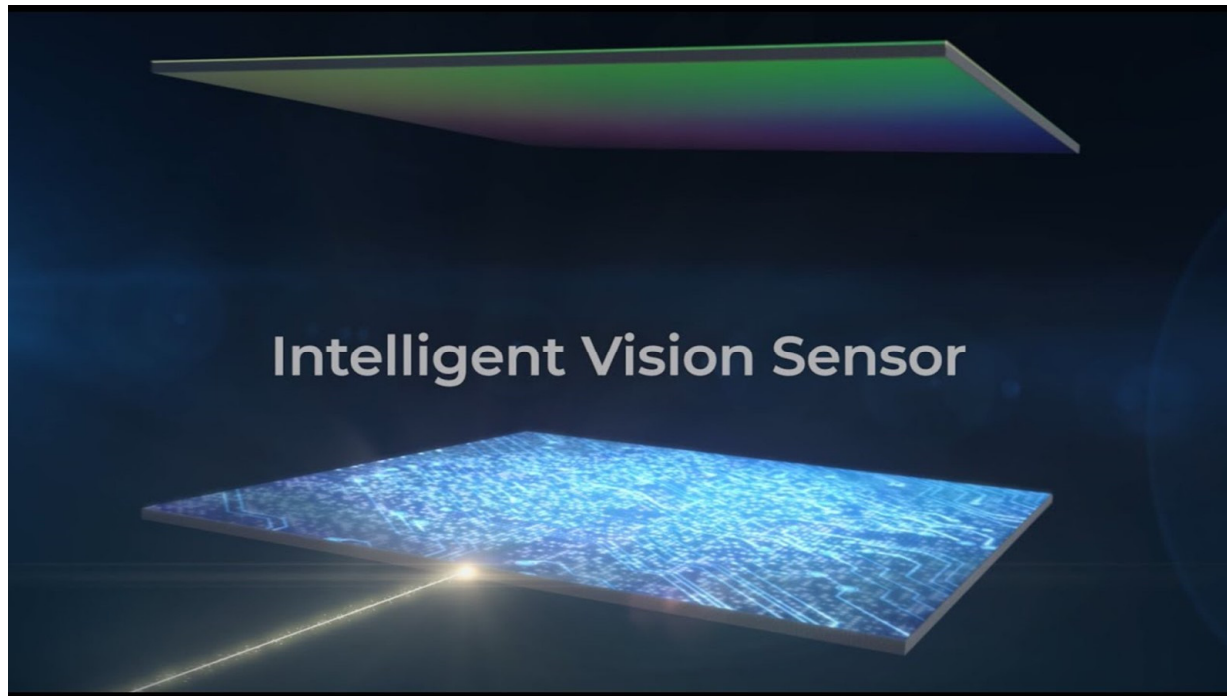
Edge AI System

- Satisfies compact, low-power, and low-latency requirements

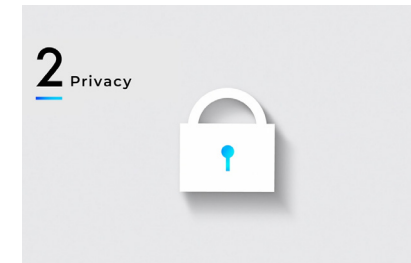


Intelligent Vision Sensor

- Eliminates requirement of high-performance processors or external memory, making it ideal for edge AI systems



Low Latency



Privacy

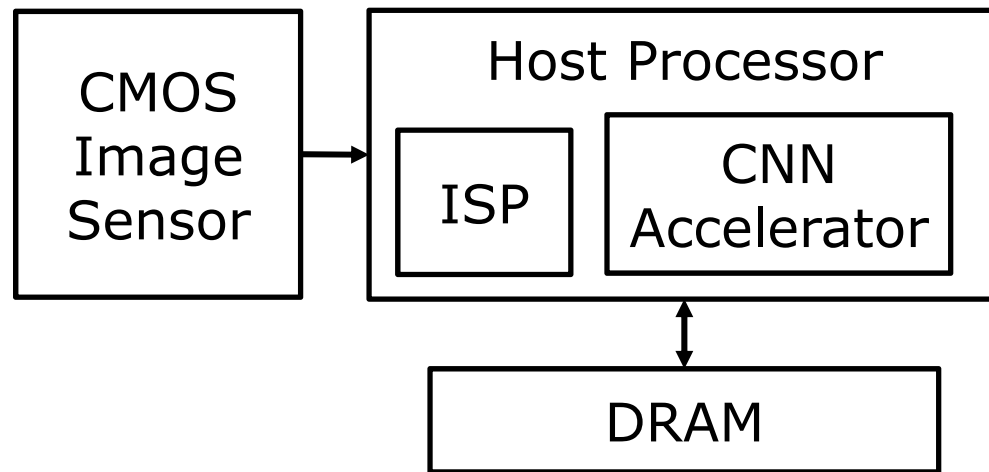


Low Power &
Low Cost

Concept of Intelligent Vision Sensor

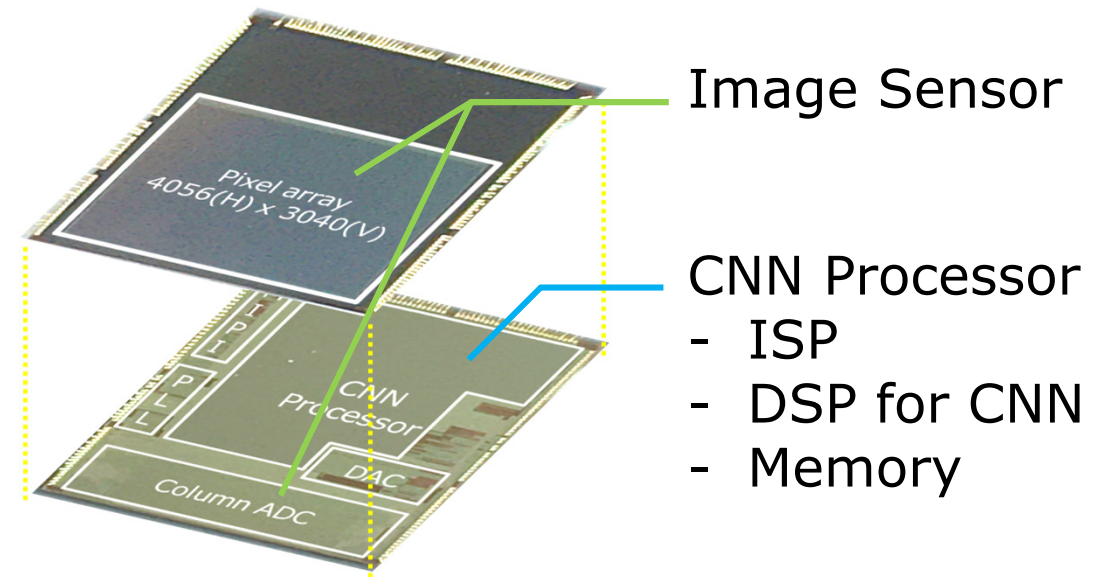
- AI processing capability on edge device solves edge AI issues

Conventional Configuration



Larger, higher power and more costly

Intelligent Vision Sensor



All functions are implemented on chip

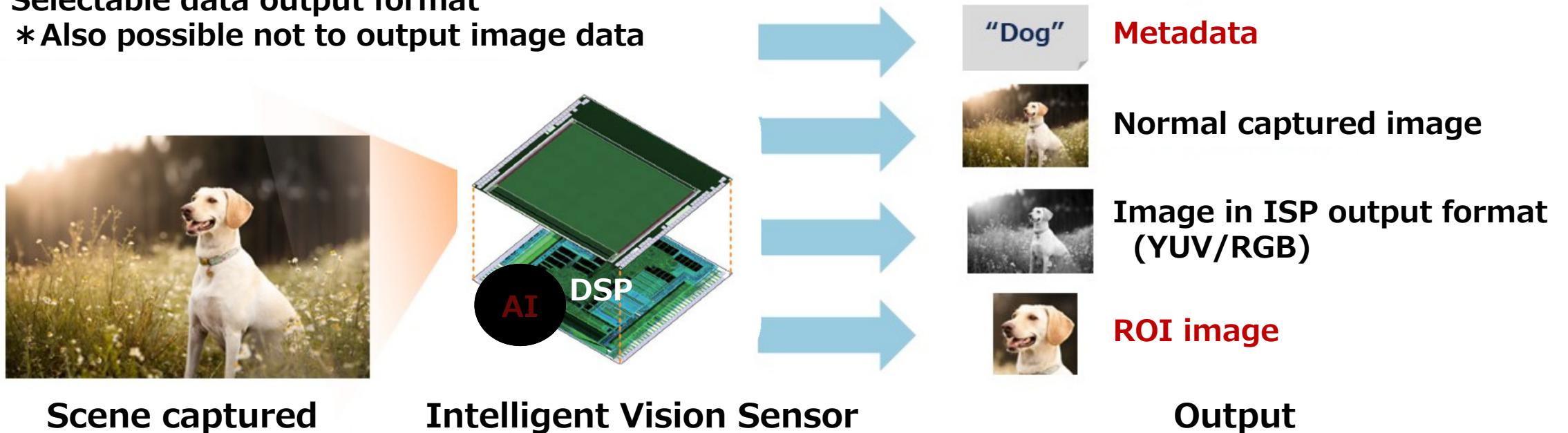
To be presented by R. Eki, ISSCC 2021

Functions of Intelligent Vision Sensor

- Equipped with DSP dedicated to AI signal processing, and memory for AI model

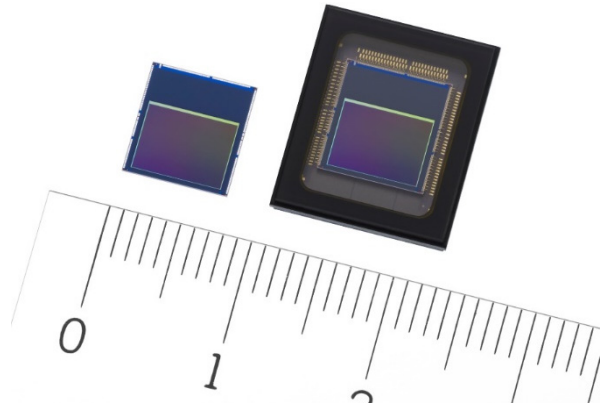
Selectable data output format

* Also possible not to output image data



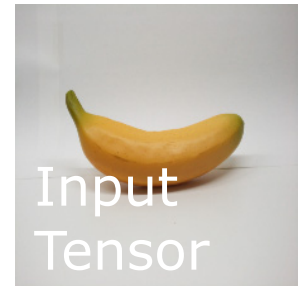
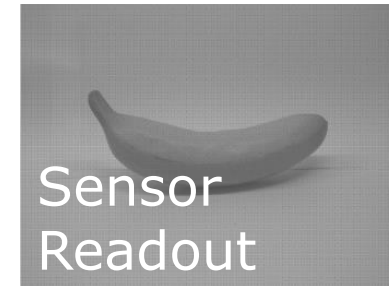
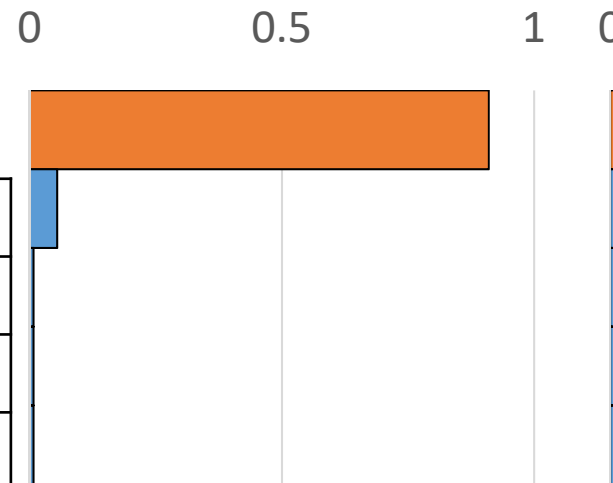
Performance Example (MobileNet v1)

- CNN inference conducted on sensor

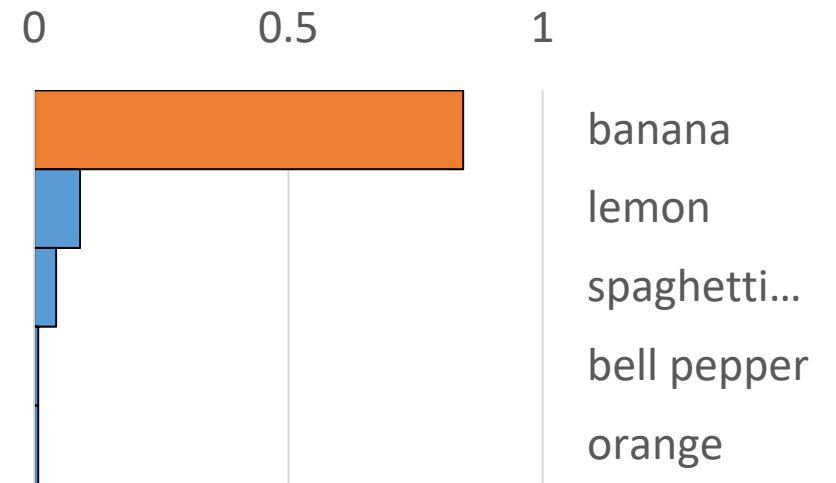


Num. pixels	12.3M (4056 x 3040)
Optical format	1/2.3 type
Pixel size	1.55 μm x 1.55 μm
Output format	Image (Bayer RAW), ISP output (YUV/RGB), Metadata, ROI

CNN Inference Results
by TensorFlow



by Intelligent Vision Sensor



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Possible Applications of Intelligent Vision Sensor

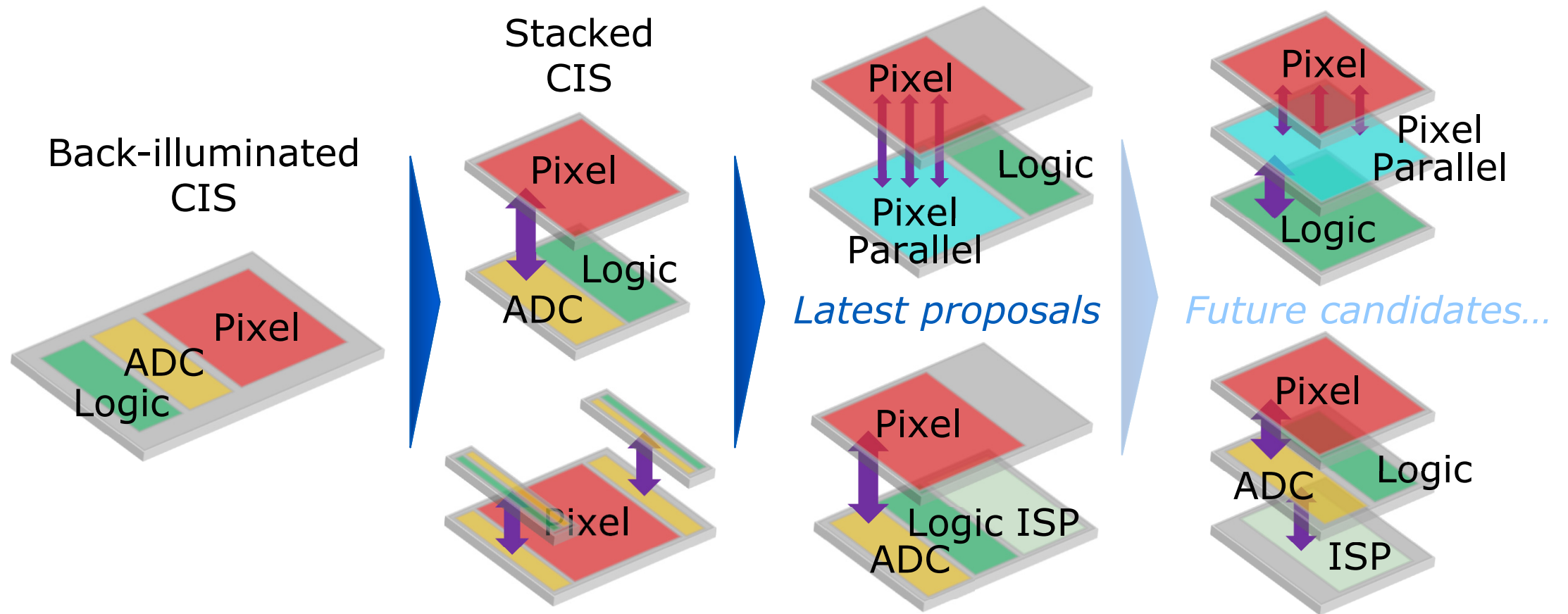
- Offering low-cost edge AI using flexible AI model

Example of camera usage
in facility



Prospect of Imaging Device using 3D Technologies

- Sensor architecture is further evolving using 3D technologies



Thank you for your attention

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