

# Using hardware transactions in the GHC runtime system<sup>\*</sup>

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## Abstract

Hardware support for transactional memory (HTM) is now mainstream with commercial offerings from both Intel and IBM. This new flexible hardware tool for synchronization gives opportunities to improve the performance of language-level synchronization and to simplify runtime system implementation. Our research has shown that concurrent data structure performance in GHC is limited when taking the simple but common approach of atomically updating a global mutable reference to the root of a pure-functional structure. Transactional memory (both the existing software implementation and our hybrid hardware/software implementation) shows much better performance as the core count grows. Our current work aims to further improve performance by reducing the overhead of transactional memory in GHC while still supporting such powerful high-level features as `retry` and `orElse`. In our talk we will share our benchmark results on a 72-thread Intel machine with HTM, details on how we have found HTM useful in the GHC runtime system, opportunities to explore other uses of HTM, and some lessons learned while working with GHC.

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