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Resource Contention-Aware Scheduling I Hardware resource sharing/contention in multi-processors

- - SMP processors share memory bus bandwidths -
 - Multi-core processors share L2 cache
 - SMT processors share a lot more stuff
- An example: on an SMP machine
 - a web server benchmark delivers around 6300 regs/sec on one processor, but only around 9500 regs/sec on an SMP with 4 processors
- Contention-reduction scheduling
 - co-scheduling tasks with complementary resource needs (a computation-heavy task and a memory access-heavy task)
- In [Fedorova et al. USENIX2005], IPC is used to distinguish computation-heavy tasks from memory 16 11/9/2009 access-heavy tasks



