Infrastructure and Methodology for Mobile SoC Modeling

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Mobile Systems Today

- Imaging
- Computer Vision
- Graphics
- Video Processing
- Stereo Acoustic
Mobile Systems Today

- Imaging
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- Graphics
- Video Processing
- Stereo Acoustic

[Diagram showing relationships between Imaging and other concepts]
Mobile Systems Today

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Image Signal Processor

[Diagram showing the flow of imaging data through the processor to the final image output]
Mobile Systems Today

Imaging

Computer Vision

Graphics

Video Processing

Stereo Acoustic

Image Signal Processor

Black Level Adjustment

Noise Reduction

White Balance

RGB to YCC Conversion

Gamma Correction

RGB Blending

CFA Interpolation

Edge Enhance

Contrast Enhance

False Chroma Suppression
Mobile Systems Today

Imaging  Computer Vision  Graphics  Video Processing  Stereo Acoustic
Mobile Systems Today

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Diagram showing relationships between Imaging, Computer Vision, Graphics, Video Processing, and Stereo Acoustic.
Mobile Systems Today

Imaging  Computer Vision  Graphics  Video Processing  Stereo Acoustic

Neural Network Engine
Mobile Systems Today

- Imaging
- Computer Vision
- Graphics
- Video Processing
- Stereo Acoustic

Neural Network Engine
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Mobile Systems Today

Imaging  Computer Vision  Graphics  Video Processing  Stereo Acoustic

3D mesh  Image Output
Mobile Systems Today

- Imaging
- Computer Vision
- Graphics
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3D mesh

Graphics Processing Unit

Image Output
Mobile Systems Today

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Graphics Processing Unit

3D mesh

Image Output

Vertex processing
Rasterization
Raster Operations
Fragment processing
Texture
Mobile Systems Today

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Mobile Systems Today

Imaging  Computer Vision  Graphics  Video Processing  Stereo Acoustic
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Video Codec
Mobile Systems Today

Imaging

Computer Vision

Graphics

Video Processing

Stereo Acoustic

Video Codec
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Video Codec

Intra-/Inter-frame Prediction Model → Residual → Transform/Quantize Residual → Entropy Encoding

Previously Coded Data
Mobile Systems Today

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[Waveform and musical notes]
Mobile Systems Today

- Imaging
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Audio Signal Processor

![Waveform and musical notes]
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Audio Signal Processor

Analog Signal
- Continuous in Time
- Continuous in Amplitude

Sample & Hold
- Sampling Frequency must be defined
- Continuous in Time
- Continuous in Amplitude

Quantization
- Discrete in Time
- Continuous in Amplitude

Encoding
- Discrete in Time
- Discrete in Amplitude

Digital Signal
- Discrete in Time
- Discrete in Amplitude
Today’s mobile systems are a collection of segregated sub-systems, each specialized for a domain.
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- Imaging
  - Image Signal Processor
- Computer Vision
  - Neural Network Engine
- Graphics
  - GPU
- Video Processing
  - Video Codec
- Stereo Acoustic
  - Audio Signal Processor
Today’s mobile systems are a collection of segregated sub-systems, each specialized for a domain.
Emerging Applications Integrate All Components

- Imaging
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Emerging Applications Integrate All Components

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Camera ➔ Headset

8
Emerging Applications Integrate All Components

Co-Optimize/Design Different Computing Domains Across the Entire SoC
Nvidia TX2 SoC
You can’t fix what you can’t measure
## Architecture Modeling Infrastructure

<table>
<thead>
<tr>
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<tbody>
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Why Do We Need Another SoC Modeling Tool?
Requirements for SoC-Level Modeling

- Do we need cycle-accurate CPU models in SoC Simulation?
- Do we need cycle-accurate GPU models in SoC Simulation?
- At what granularity should we model the SoC?
- What are evaluation metrics should we care about?
- What IP blocks should we support, and how do we support new IP blocks?
- First-order bottleneck analysis vs. detailed perf. model
Different Modeling Levels and Strategies

- Hardware Modeling
  - Analytical Model
  - Simulation Model
- Task-level Modeling
  - SoC-level tasks (case-study: continuous vision)
  - IP-level tasks (case-study: DNN accelerator)
Rest of the Agenda

- **Introduction and Welcome (Yuhao Zhu, Rochester)**
- Platform Architecture Modeling Tutorial (Jun Qi, Synopsys)
- Platform Architecture Simulation Model of Gables (Xiaoyang Li, Synopsys)
- Task-level Modeling: A Continuous Vision Case-Study (Yiming Gan, Rochester)
- Joint Optimization of Hardware and Compiler -- Modeling AI Accelerators using Platform Architect (Xiaoyang Li, Synopsys)