CSC 252: Computer Organization
Spring 2018: Lecture 16

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University of Rochester

Action Items:
• Programming Assignment 4 is out
Announcement

• Programming Assignment 4 is out
  • Main assignment due on 11:59pm, Monday, April 2.
Last Lecture: Memory Hierarchy

- Fundamental tradeoff
  - Fast memory: small
  - Large memory: slow
Locality

- **Principle of Locality:** Programs tend to use data and instructions with addresses near or equal to those they have used recently.
Locality

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• **Temporal locality:**
  • Recently referenced items are likely to be referenced again in the near future
Locality

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• **Temporal locality:**
  - Recently referenced items are likely to be referenced again in the near future

• **Spatial locality:**
  - Items with nearby addresses tend to be referenced close together in time
Locality Example

- **Data references**
  - **Spatial** Locality: Reference array elements in succession (stride-1 reference pattern)
  - **Temporal** Locality: Reference variable sum each iteration.

- **Instruction references**
  - **Spatial** Locality: Reference instructions in sequence.
  - **Temporal** Locality: Cycle through loop repeatedly.

```c
sum = 0;
for (i = 0; i < n; i++)
    sum += a[i];
return sum;
```
Example Memory Hierarchy

L0: Regs
- CPU registers hold words retrieved from the L1 cache.

L1: L1 cache (SRAM)
- L1 cache holds cache lines retrieved from the L2 cache.

L2: L2 cache (SRAM)
- L2 cache holds cache lines retrieved from L3 cache

L3: L3 cache (SRAM)
- L3 cache holds cache lines retrieved from main memory.

L4: Main memory (DRAM)
- Main memory holds disk blocks retrieved from local disks.

L5: Local secondary storage (local disks)
- Local disks hold files retrieved from disks on remote servers.

L6: Remote secondary storage (e.g., Web servers)
- Larger, slower, and cheaper (per byte) storage devices

Smaller, faster, and costlier (per byte) storage devices
How Things Have Progressed

<table>
<thead>
<tr>
<th>Year</th>
<th>Low-Mid Range</th>
<th>RF</th>
<th>Cache</th>
<th>Memory</th>
<th>Disk</th>
</tr>
</thead>
<tbody>
<tr>
<td>1995</td>
<td>200B 5ns</td>
<td></td>
<td>64KB 10ns</td>
<td>32MB 100ns</td>
<td>2GB 5ms</td>
</tr>
<tr>
<td></td>
<td>Hennessy &amp; Patterson,</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Computer Arch., 1996</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2009</td>
<td>~200B 0.33ns</td>
<td></td>
<td>8MB 0.33ns</td>
<td>4GB &lt;100ns</td>
<td>750GB 4ms</td>
</tr>
<tr>
<td></td>
<td><a href="http://www.dell.com">www.dell.com</a>, $449</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>including 17&quot; LCD</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>flat panel</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2015</td>
<td>~200B 0.33ns</td>
<td></td>
<td>8MB 0.33ns</td>
<td>16GB &lt;100ns</td>
<td>256GB 10us</td>
</tr>
</tbody>
</table>

|            | mid range              |       |          |           |         |
Cache Illustrations

CPU

Memory (big but slow)
Cache Illustrations

CPU

Cache (small but fast)

8 9 14 3

Memory (big but slow)

0 1 2 3
4 5 6 7
8 9 10 11
12 13 14 15

Memory (big but slow)
Cache Illustrations

CPU

Cache (small but fast)

Memory (big but slow)
Cache Illustrations

CPU

Cache (small but fast)

Memory (big but slow)
Cache Illustrations

CPU

Cache (small but fast)

Memory (big but slow)

0 1 2 3
4 5 6 7
8 9 10 11
12 13 14 15

- Memory (big but slow)
- Cache (small but fast)
- CPU

- Memory contains data that is accessed frequently by the CPU.
- Cache is a smaller, faster version of memory.
- The CPU accesses data from cache first, then from memory if the data is not in cache.

Example:
- The CPU needs to access data with the value 9.
- If the data is in the cache, the CPU accesses it quickly.
- If the data is in memory, the CPU accesses it more slowly.

Key:
- Red squares indicate data items in cache.
- White squares indicate data items in memory.
Cache Illustrations

CPU

Cache (small but fast)

Memory (big but slow)
Cache Illustrations

CPU

Cache (small but fast)

Memory (big but slow)
Cache Illustrations

CPU

Cache (small but fast)

Memory (big but slow)
Cache Illustrations: Hit

CPU

Cache (small but fast)

8  9  14  3

Memory (big but slow)

0  1  2  3
4  5  6  7
8  9 10 11
12 13 14 15
Cache Illustrations: Hit

Data in address b is needed

CPU

Cache (small but fast)

Request: 14

Memory (big but slow)
Cache Illustrations: Hit

Data in address b is needed

Address b is in cache: Hit!
Cache Illustrations: Miss

CPU

Cache (small but fast)

Memory (big but slow)
Cache Illustrations: Miss

CPU

Request: 12

Cache (small but fast)

Memory (big but slow)
Cache Illustrations: Miss

Request: 12

Data in address b is needed

Address b is not in cache: Miss!
Cache Illustrations: Miss

CPU

Cache (small but fast)

Request: 12

Data in address b is needed

Address b is not in cache: Miss!

Address b is fetched from memory

Memory (big but slow)
Cache Illustrations: Miss

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CPU

Cache (small but fast)

8 9 14 3

12

Request: 12

Data in address b is needed

Address b is not in cache: Miss!

Address b is fetched from memory

Memory (big but slow)

0 1 2 3

4 5 6 7

8 9 10 11

12 13 14 15

...
Cache Illustrations: Miss

- **CPU**
- **Cache** (small but fast)
- **Memory** (big but slow)

**Request:** 12

Data in address \(b\) is needed

Address \(b\) is not in cache: **Miss!**

Address \(b\) is fetched from memory

Address \(b\) is stored in cache
Cache Hit Rate

• Cache hit is when you find the data in the cache
• Hit rate indicates the effectiveness of the cache

\[
\text{Hit Rate} = \frac{\# \text{ Hits}}{\# \text{ Accesses}}
\]
Two Fundamental Issues in Cache Management

• Placement
  • Where in the cache is data placed?
  • Or more importantly, how can I find my data?
  • Random placement? Pros vs. cons

• Replacement
  • Given more than one location to place, where is data placed?
  • Or, what to kick out?
Cache Management: Explicit

• Under explicit software control.
• Requirements:
  • Cache and memory have different address spaces
  • Different memory access instructions for cache and memory
• Often hard/impossible to get right
Cache Management: Explicit

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- Examples of software-managed cache
  • Sony Cell Broadband Engine (PS3): Local store
  • DSPs: Scratchpad memory
  • GPUs: “Shared memory”
  • Stream Processors: Stream register file
Want Automatic Management

• Software-managed cache is nice, but
  • explicit management is painful
  • often cannot tell statically what will be reused
  • code portability suffers too
• Caches are thus mostly hardware-managed
  • When we say cache today, it almost always means hardware-managed cache
  • Software-managed cache is often called scratchpad memory
  • Cray never believed in hardware-managed cache ("Caches are for wimps!")

Baseline Cache & Memory

- 4 cache locations
  - Also called cache-line
  - Every location has a valid bit
- 16 memory locations
  - For now, assume cache location size == memory location size
  - Assume each memory location can only reside in one cache-line
  - Cache is smaller than memory (obviously)
  - Thus, not all memory locations can be cached at the same time
Cache Placement

Cache

Memory

CA

cache func

addr

00
01
10
11

0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
Cache Placement

- Use memory address as a name
- Apply a function to the name to generate a cache address to access
- What are reasonable functions?
Function to Address Cache

• Simplest function is a subset of address bits
  • CA = ADDR[3], ADDR[2]
  • CA = ADDR[3], ADDR[1]
  • CA = ADDR[3], ADDR[0]
  • CA = ADDR[2], ADDR[1]
  • CA = ADDR[2], ADDR[0]
  • CA = ADDR[1], ADDR[0]

• Six combinations in total
  • CA = ADDR[3], ADDR[2]
  • CA = ADDR[3], ADDR[1]
  • CA = ADDR[3], ADDR[0]
  • CA = ADDR[2], ADDR[1]
  • CA = ADDR[2], ADDR[0]
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• Direct-Mapped Cache
  • CA = ADDR[1], ADDR[0]
Direct-Mapped Cache
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- CA = ADDR[1], ADDR[0]
- Always use the lower order address bits
Direct-Mapped Cache

• Direct-Mapped Cache
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• Multiple addresses can be mapped to the same location
  • E.g., 0010 and 1010
Direct-Mapped Cache

- **Direct-Mapped Cache**
  - $CA = ADDR[1], ADDR[0]$
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- **Multiple addresses can be mapped to the same location**
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- **How do we differentiate between different memory locations that are mapped to the same cache location?**
  - Add a tag field for that purpose
  - ADDR[3] and ADDR[2] in this particular example
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  • Add a tag field for that purpose
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Example: Direct-Mapped Cache

```
for (i = 0; i < 4; ++i) {
    A += mem[i];
}

for (i = 0; i < 4; ++i) {
    B *= (mem[i] + A);
}
```

- Assume mem == 0b1000
- Read 0b1000
- Read 0b1001
- Read 0b1010
- Read 0b1011
- Read 0b1000; cache hit?
Example: Direct-Mapped Cache

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- Read 0b1010
- Read 0b1011
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• Read 0b1011
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- Read 0b1000
- Read 0b1001
- Read 0b1010
- Read 0b1011
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• Read 0b1010
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One Possible Direct-Mapped Cache Implementation

- Cache state is RAM!
- Implement cache as a single SRAM
- Need appropriate comparators
- Memory is implemented as a DRAM
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One Possible Direct-Mapped Cache Implementation

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- Implement cache as a single SRAM
- Need appropriate comparators
- Memory is implemented as a DRAM
Conflicts

Cache

Memory

addr[3:2] = addr[1:0] 

addr

addr[1:0] = Hit?

0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

a
b
c
d
Conflicts

Assume the following memory access stream:

```
0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111
```

```
a b c d
```
Conflicts

Assume the following memory access stream:

- Read 1000
Assume the following memory access stream:

- Read 1000
Assume the following memory access stream:

- Read 1000
- Read 1001
Conflicts

Assume the following memory access stream:
- Read 1000
- Read 1001
Assume the following memory access stream:

- Read 1000
- Read 1001
- Read 1010
Assume the following memory access stream:

- Read 1000
- Read 1001
- Read 1010
Assume the following memory access stream:

- Read 1000
- Read 1001
- Read 1010
- Read 1101 (kick out 1001)
Assume the following memory access stream:

- Read 1000
- Read 1001
- Read 1010
- Read 1101 (kick out 1001)
  - addr[1:0]: 01
Conflicts

Assume the following memory access stream:

- Read 1000
- Read 1001
- Read 1010
- Read 1101 (kick out 1001)
  - addr[1:0]: 01
  - addr[3:2]: 11
Assume the following memory access stream:

- Read 1000
- Read 1001
- Read 1010
- Read 1101 (kick out 1001)
  - addr[1:0]: 01
  - addr[3:2]: 11
Assume the following memory access stream:

- Read 1000
- Read 1001
- Read 1010
- Read 1101 (kick out 1001)
  - addr[1:0]: 01
  - addr[3:2]: 11
- Read 1001 -> Miss!
Assume the following memory access stream:

- Read 1000
- Read 1001
- Read 1010
- Read 1101 (kick out 1001)
  - addr[1:0]: 01
  - addr[3:2]: 11
- Read 1001 -> Miss!

Why? Each memory location is mapped to only one cache location.
Sets

• Each cacheable memory location is mapped to a set of cache locations
• A set is one or more cache locations
• Set size is the number of locations in a set, also called associativity
2 Way Set Associative
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- 2 sets, each set has two entries
2 Way Set Associative

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- Only need one bit, addr[0] to index into the cache now
2 Way Set Associative

- 2 sets, each set has two entries
- Only need one bit, addr[0] to index into the cache now
- Correspondingly, the tag needs 3 bits: Addr[3:1]

```
0 1

Set 0  Set 1
```
2 Way Set Associative

- 2 sets, each set has two entries
- Only need one bit, addr[0] to index into the cache now
- Correspondingly, the tag needs 3 bits: Addr[3:1]
- Either entry can store any address that gets mapped to that set
2 Way Set Associative

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- Only need one bit, \text{addr}[0] to index into the cache now
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- Now with the same access stream:
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- Now with the same access stream:
  - Read 1000
  - Read 1001
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- Now with the same access stream:
  - Read 1000
  - Read 1001
  - Read 1010
  - Read 1101 (1001 can still stay)
2 Way Set Associative

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- Only need one bit, $\text{addr}[0]$ to index into the cache now
- Correspondingly, the tag needs 3 bits: $\text{Addr}[3:1]$
- Either entry can store any address that gets mapped to that set
- Now with the same access stream:
  - Read 1000
  - Read 1001
  - Read 1010
  - Read 1101 (1001 can still stay)
  - Read 1001 -> Hit!
4 Way Set Associative

- One single set that contains all the cache locations
- Also called Fully-Associative Cache
- Every entry can store any cache-line that maps to that set
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Assuming the same access stream
4 Way Set Associative

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Assuming the same access stream
- Read 1000
4 Way Set Associative

- One single set that contains all the cache locations
- Also called Fully-Associative Cache
- Every entry can store any cache-line that maps to that set

Assuming the same access stream
- Read 1000
- Read 1001
4 Way Set Associative

- One single set that contains all the cache locations
- Also called Fully-Associative Cache
- Every entry can store any cache-line that maps to that set

Assuming the same access stream
- Read 1000
- Read 1001
- Read 1010
4 Way Set Associative

- One single set that contains all the cache locations
- Also called Fully-Associative Cache
- Every entry can store any cache-line that maps to that set

Assuming the same access stream
- Read 1000
- Read 1001
- Read 1010
- Read 1101
4 Way Set Associative

- One single set that contains all the cache locations
- Also called Fully-Associative Cache
- Every entry can store any cache-line that maps to that set

Assuming the same access stream
- Read 1000
- Read 1001
- Read 1010
- Read 1101
- Read 1001 -> **Hit!**
Associative verses Direct Mapped Trade-offs
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- Direct-Mapped cache
  - Generally lower hit rate
  - Simpler, Faster
Associative verses Direct Mapped Trade-offs

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- Direct-Mapped cache
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- Associative cache
  - Generally higher hit rate. Better utilization of cache resources
  - Slower. Why?

```
<table>
<thead>
<tr>
<th>addr[3:2]</th>
<th>a</th>
<th>1</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>b</td>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>c</td>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>d</td>
<td>1</td>
<td>10</td>
</tr>
</tbody>
</table>

For example:
- Address 00: Hit
- Address 01: Miss
- Address 10: Hit
- Address 11: Miss

0  | a  | 1  | 101 |
1  | b  | 1  | 101 |
10 | c  | 1  | 100 |
11 | d  | 1  | 100 |
```
Associative verses Direct Mapped Trade-offs

• Direct-Mapped cache
  • Generally lower hit rate
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• Associative cache
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```
<table>
<thead>
<tr>
<th>addr[1:0]</th>
<th>addr[3:2]</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>a 1</td>
</tr>
<tr>
<td>01</td>
<td>b 1</td>
</tr>
<tr>
<td>10</td>
<td>c 1</td>
</tr>
<tr>
<td>11</td>
<td>d 1</td>
</tr>
</tbody>
</table>
```

```
<table>
<thead>
<tr>
<th>addr[0]</th>
<th>addr[3:2]</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>a 1</td>
</tr>
<tr>
<td>11</td>
<td>b 1</td>
</tr>
<tr>
<td>01</td>
<td>c 1</td>
</tr>
<tr>
<td>11</td>
<td>d 1</td>
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```
Associative verses Direct Mapped Trade-offs

- **Direct-Mapped cache**
  - Generally lower hit rate
  - Simpler, Faster

- **Associative cache**
  - Generally higher hit rate. Better utilization of cache resources
  - Slower. Why?

```
  addr[1:0]  ==  Hit?
    |      |
  addr[3:2]  ==
    |      |
  addr[0]     ==
    |      |
  addr[3:1]   ==
```

```
  addr[1:0]  ==  Hit?
    |      |
  addr[3:2]  ==
    |      |
  addr[0]     ==
    |      |
  addr[3:1]   ==
```

```
00
  a  1  10
  b  1  10
  c  1  10
  d  1  10
```

```
01
  a  1  101
  b  1  101
  c  1  100
  d  1  100
```
Associative verses Direct Mapped Trade-offs

- Direct-Mapped cache
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<table>
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<tr>
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<th>addr[3:2]</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
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</tr>
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</tr>
<tr>
<td>10</td>
<td>c 1 10</td>
</tr>
<tr>
<td>11</td>
<td>d 1 10</td>
</tr>
</tbody>
</table>

- addr[0]
  - addr[3:1]
  - Hit?

- addr
  - addr[3:2]
  - Hit?

- Or
  - addr[0]
  - addr[3:1]
  - Hit?
Cache Access Summary (So far…)

- Assuming $b$ bits in a memory address
- The $b$ bits are split into two halves:
  - Lower $s$ bits used as index to find a set. Total sets $S = 2^s$
  - The higher $(b - s)$ bits are used for the tag
- Associativity $n$ is independent of the the split between index and tag
Locality again

- So far: temporal locality
- What about spatial?
- Idea: Each cache location (cache line) store multiple bytes
Cache-Line Size of 2

Cache

Memory


0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

a
b
c
d
Cache-Line Size of 2

Cache

Memory


00
01
10
11

0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

a
b
c
d
Cache-Line Size of 2

Cache

Memory

- Read 1000
Cache-Line Size of 2

- Read 1000
- Read 1001 (Hit!)
Cache-Line Size of 2

- Read 1000
- Read 1001 (Hit!)
- Read 1010
Cache-Line Size of 2

- Read 1000
- Read 1001 (Hit!)
- Read 1010
- Read 1011 (Hit!)
Cache Access Summary

- Assuming $b$ bits in a memory address
- The $b$ bits are split into three fields:
  - Lower $l$ bits are used for byte offset within a cache line. Cache line size $L = 2^l$
  - Next $s$ bits used as index to find a set. Total sets $S = 2^s$
  - The higher $(b - l - s)$ bits are used for the tag
- Associativity $n$ is independent of the the split between index and tag

<table>
<thead>
<tr>
<th>Memory Address</th>
<th>$b$</th>
<th>$l+s$</th>
<th>$l$</th>
<th>$0$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>tag</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>index</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>offset</td>
<td></td>
</tr>
</tbody>
</table>
Handling Reads
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- Read miss: Put into cache
Handling Reads

• Read miss: Put into cache
  • Any reason not to put into cache?
Handling Reads

- Read miss: Put into cache
  - Any reason not to put into cache?
- Read hit: Nothing special. Enjoy the hit!
Handling Writes (Hit)

• Intricacy: data value is modified!
• Implication: value in cache will be different from that in memory!

• When do we write the modified data in a cache to the next level?
  • Write through: At the time the write happens
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  • + Can consolidate multiple writes to the same block before eviction. Potentially saves bandwidth between cache and memory + saves energy
  • - Need a bit in the tag store indicating the block is “dirty/modified”
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• Write-through
  • + Simpler
  • + Memory is up to date
  • - More bandwidth intensive; no coalescing of writes
  • - Requires transfer of the whole cache line (although only one byte might have been modified)
Handling Writes (Miss)

• Do we allocate a cache line on a write miss?
  • Write-allocate: Allocate on write miss
  • Non-Write-Allocate: No-allocate on write miss

• Allocate on write miss
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• Non-allocate
  • + Conserves cache space if locality of writes is low (potentially better cache hit rate)
Instruction vs. Data Caches

- Separate or Unified?
Instruction vs. Data Caches

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• Unified:
Instruction vs. Data Caches

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  • - Inst and Data are accessed in different places in the pipeline.
    Where do we place the unified cache for fast access?

• First level caches are almost always split
  • Mainly for the last reason above

• Second and higher levels are almost always unified
Eviction/Replacement Policy

• Which cache line should be replaced?
Eviction/Replacement Policy

• Which cache line should be replaced?
  • Direct mapped? Only one place!
Eviction/Replacement Policy

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  • Ideally: Replace the cache line that’s least likely going to be used again
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  • If all are valid, consult the replacement policy
  • Randomly pick one???
  • Ideally: Replace the cache line that’s least likely going to be used again
    • Approximation: Least recently used (LRU)
Implementing LRU

• Idea: Evict the least recently accessed block
• Challenge: Need to keep track of access ordering of blocks
• Question: 2-way set associative cache:
  • What do you need to implement LRU perfectly? One bit?

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Address stream:
• Hit on 0
• Hit on 1
• Miss, evict 0
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Implementing LRU

Cache Lines

LRU index (2 bits)

Address stream:
- Hit on 0
- Hit on 2
- Hit on 3
- Miss, evict 1
Implementing LRU

• Question: 4-way set associative cache:
  • What do you need to implement LRU perfectly?
  • Will the same mechanism work?

Address stream:
• Hit on 0
• Hit on 2
• Hit on 3
• Miss, evict 1

Cache Lines

  0  1  2  3

LRU index (2 bits)

  1
Implementing LRU

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LRU index (2 bits)

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- 2
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**LRU index (2 bits)**

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  • Google Pseudo-LRU

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What to update now???
General Rule: Bigger == Slower

CPU ← Cache $ → Memory
General Rule: Bigger == Slower

- How big should the cache be?
  - Too small and too much memory traffic
  - Too large and cache slows down execution (high latency)
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  • Today’s processors typically have 3 cache levels
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Summary

• Assumptions:
  • memory access (~100ns) >> cache access (~1ns)
    • cache smaller, faster, more expensive than memory
  • Programs exhibit *temporal locality*
    • if an item is referenced, it will tend to be referenced again soon
  • Programs exhibit *spatial locality*
    • If an item is referenced, the next item in memory is likely to be accessed soon